Applied Thermal Engineering 214 (2022) 118845

Contents lists available at ScienceDirect

Applied Thermal Engineering

journal homepage: www.elsevier.com/locate/apthermeng

Research Paper

A system level optimization of on-chip thermoelectric cooling via Taguchi-Grey method

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ARTICLE INFO

Keywords:
Thin-film thermoelectric cooler
3D electronic package
Hotspot cooling
Integrated design
Taguchi method
Grey relational analysis

ABSTRACT

In this paper, a framework for the system level optimization of the thin-film thermoelectric cooler (TFTEC) in 3D electronic packaging is developed based on Taguchi-Grey method. The influences of the size effect, the geometric effect, the parasitic effect and the localized hotspot are comprehensively considered. An L_{25} (5^6) orthogonal array is employed to assess the influences of the leg height, the fill-ratio, the electrode height, the gap distance, the hotspot size and the hotspot heat flux on the passive and active cooling effects of the TFTEC. The results show that the electrode height, acting as the primary factor, contributes 45.5% and 45.3% on the passive cooling and active cooling, respectively. The contribution ratios of hotspot size and hotspot heat flux to passive cooling reach 21.4% and 14.7%, respectively. The contribution ratios of leg height and gap distance to active cooling reach 25.7% and 18.8%, respectively. The optimum design factors for maximizing the cooling effects are also approached by the Grey relational analysis. A passive cooling of 16.82 °C and a maximum active cooling of 12.29 °C are achieved, leading to a total localized cooling of 29.11 °C for a chip hotspot.

1. Introduction

With the continuous advancement of microelectronic technology, electronics are moving toward miniaturization and high packaging density. The resulting high power density elevates temperature and accelerates the risk of reliability failure. As such, the thermal issues are always considered a vitally important stressor in the robustness design of electronics [1]. This problem has exacerbated for the new generation of wide bandgap semiconductor devices, due to their superior performance which owns high temperature operating points (200–250 °C [2]) and high chip heat fluxes (>1 kW/cm^2 [3]). Besides, the heat flux distributions on such devices can be highly non-uniform, i.e. hotspots, which not only degrade the performance, but also deteriorate the reliability. To date, conventional cooling methods mainly include heat pipes[4], micro-channels [5], spray cooling [6] and jet impingement [7], which are often suffered from over-designed, low reliability, expensive, bulky, and are restricted by specific application scenarios. To improve the performance and reliability of cutting edge electronics, the compact thermal management solutions for hotspot cooling with minimal energy consumption are urgently required.

Thermoelectric cooler (TEC) is a solid-state heat pump that can provide site-specific and on-demand cooling for hotspot removal of electronic devices [8]. To achieve high heat flux removal ability, the dimensionless figure of merit (ZT) of thermoelectric (TE) material needs to be large enough. Recently, significant progress has been made in using nanostructured materials, such as thin-film superlattice [9], quantum dot superlattice thick films [10], and nanocomposites [11]. These TE materials with high ZT values can extend their applications in scenarios with high heat fluxes. However, the transformation of these laboratory breakthroughs into commercial solutions is still in its infancy. TE geometry and structural optimization is a vital research area that has been extensively explored due to significant performance enhancement achieved. Many researchers are now focusing on this area, therefore, the amount of available literature on this field has increased dramatically in

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https://doi.org/10.1016/j.applthermaleng.2022.118845
Received 22 March 2022; Received in revised form 8 June 2022; Accepted 11 June 2022
Available online 15 June 2022

recent years.

Hao et al. [12] introduced a typical TEC model and constructed the overall heat transfer and electric-heat conversion model for the overall geometric optimization of the TEC. Luo et al. [13] performed a parametric study to predict the performance of TE devices by using numerical simulations. The influences of leg height, cross-sectional area, number of couples, ceramic plates and fillers were investigated. Gong et al. [14] performed three-dimensional (3D) finite element simulations on the optimal design of the compact TEC. The results showed that the Joule heat played a vital role in the performance and operational reliability of the TEC. Qiu et al. [15] developed 3D numerical simulations for a sandwich-structured TEC with non-constant and constant cross sections by using finite element method. Meng et al. [16] employed a combination of non-dominated Sorting Genetic Algorithm II (NSGA-II) and 3D numerical simulations to design the optimal structure of a separate and combined two-stage TEG-TECs. Khanh et al. [17] proposed a method using simulated annealing (SA) to optimize the dimensions of TECs and maximize the rate of refrigeration. Soprani et al. [18] used topology optimization combined with 3D finite element method to optimize the integration setup of a commercial TEC. Heghmanns et al. [19] introduced a multi-objective optimization program based on genetic algorithm to solve the target optimization problem of TE modules under actual boundary conditions. Kishore et al. [20] conducted an optimization study on a TEC by using Taguchi method. It was found that Taguchi method was enabled to provide optimum or near-optimum TEC configuration using only 25 experimental runs against 3125 runs needed by the conventional experimental techniques. For more information on TE geometry and structural optimization, interested readers can refer to the recent review by Shittu et al [21]. The review demonstrated the 3D finite optimization and multi-objective optimization methods in detail.

Since the cooling flux density is inversely proportional to the thickness of the TE material, thin-film TECs (TFTECs) are developed to increase the cooling flux density and achieve excellent local cooling capacity per unit area and volume [22]. TFTECs are emerging as a viable option for the on-chip thermal management of electronics and microprocessors. Venkatasubramanian et al. [9] reported a superlattice-based TFTEC exhibited excellent cooling capacity of 32 K near room temperature and had the potential to pump up to 700 W/cm^2 of heat flux. Chowdhury et al. [8] reported localized cooling as much as 15 °C at a high heat flux of 1300 W/cm^2 in a silicon chip by integrating multiple Bi_2Te_3 superlattice-based TFTECs. This on-chip cooling technology offered the possibility to enable a wide range of thermally limited applications. Corbett el al. [23] proposed an electrodeposited Bi_2Te_3-based TFTEC capable of pumping a maximum heat flux of 720 W/cm^2 at zero temperature difference, and a net cooling of 4.4 K can be obtained.

Geometry and structural optimization of TFTEC is also a critical issue limiting its industrial application. Many efforts have been devoted to this area to enhance the cooling performance of the TFTEC. Manno et al. [24] investigated the effect of etching micro-contact structure on the cooling performance of TFTEC. For a hotspot with a heat flux density of 2.5 kW/cm^2, the TE cooling can greatly improve the uniformity of the chip temperature distribution and reduce the temperature rise of the hotspots to less than 6 K. Redmond et al. [25] numerically investigated the hotspot cooling efficiency of a 2D electronic package with two dies and four ultrathin superlattice-based TFTECs. A passive cooling up to 9 °C and a steady-state active cooling of 5.6 °C were observed at the hotspot location. Choday et al. [26] compared the performance of Bi_2Te_3/Sb_2Te_3 superlattice-based TFTECs integrated directly on the silicon die with those that are attached to the heat spreader of the package. Finite element simulations showed that a hotspot with a heat flux of 200 W/cm^2 can be cooled by 19 °C. Wang et al. [27] proposed an equivalent thermal resistance model of TECs to evaluate the influence of a different package structure on the steady-state system temperature. The results showed that the chip temperature with integrated TECs package can be reduced by 10.6 °C. Yuruker et al. [28] proposed an overall optimization analysis method for TFTECs to optimize the thickness and current of the TE elements. The result showed that there was an optimal thickness and a corresponding optimal current to maximize the temperature drop. Nimmagadda et al. [29] recently reviewed on-chip cooling TFTEC, which covered TE on-chip cooling materials and practical cases. They discussed the reliability issues that affected the on-chip cooling of the TFTEC, which was largely depended on the device configuration, parasitic effects, and operating conditions. Further, Wang et al. [30] investigated the transient interlaminar thermal stress in multilayer materials in TFTEC and found that the interlaminar thermal stress at the free end of the TE material showed significant stress concentration. Yan et al. [31] developed a long-delay pump–probe measurement tool to characterize thermal transport and thermal stress in TFTEC. Chen et al. [32] suggested that proper device design based on state-of-the-art TE materials, such as device geometry design, contact interface engineering, and TE and microchip integration design, can further expand the application potential of TFTECs for finite cooling requirement of microchips. Consequently, an intelligent TFTEC deployment strategy must be designed at the system level to achieve a practical packaged TFTEC-based cooling solution. The strategy should overcome the performance challenges posed by device geometry design and package integration, while addressing fundamental problem of overall energy efficiency.

The economic viability of TFTEC packages for chip hotspot cooling involves numerous challenges and engineering trade-offs. Rangarajan et al. [33] proposed an optimization framework based on genetic algorithm approach that enabled system-level optimization of on-chip TE cooling in commercial microprocessor packages. The optimization found that at the thermal design power provided by each core, the resulting cooling was up to 3 °C and the energy efficiency was improved by about 11%. Kattan et al. [34] demonstrated a TFTEC-based energy-efficient thermal management technology for mobile phone processors. The results showed that the TFTEC can reduce the peak temperature of the chip by 24 °C and the average temperature by 10 °C, while the cost was only 67.5 mW. On the other hand, TFTEC can be used to compensate 89% of the required cooling energy by harvesting energy. It is worth mentioning that, in addition to being applied to chip cooling, the system level optimization framework for TFTECs can also play a role in wearable personal thermal management applications [35], as well as multi-scale uses such as power supplies with wearable electronics [36], industrial waste heat recovery devices [37], heat flux sensors [38], etc.

Motivated by the development of TFTEC, optimizing the geometric of TFTEC is of vital importance to improve its cooling performance. However, the influence of thermal and electrical parasitic effects introduced by the heterogeneous interfaces on the cooling performance has increased sharply [39]. Besides, during the on-chip cooling service of the TFTEC, the heat accumulation caused by the irreversible effects such as the Joule heat and the Fourier heat would cause serious performance degradation and reliability failure [14,40]. Furthermore, the integrated TFTEC generally exhibits a certain passive cooling effect in addition to active cooling performance. The difference between the two cooling modes makes their influence mechanisms different, which may lead to different optimal design configurations. Therefore, system-level optimization requires a holistic approach. However, there are few studies on system-level optimization involving these aspects simultaneously.

As mentioned above, there are multiple methods that can be used to optimize the performance of the TFTEC on-chip cooling system. However, when the number of design factors is sizeable, the experimental design would encounter some challenges [41]. Once all the experiments are carried out, the investigation would be time-consuming. In addition, it is difficult to determine the effect of each parameter on physical phenomena and interpret the results. Taguchi method has been widely used in the design and analysis of TE devices [42–45] and other energy systems [46,47], and has proven to be a powerful tool due to its simplicity and robustness. Taguchi method can identify important design parameters and determine optimal design parameters under

different conditions, which can greatly reduce time and effort. However, Taguchi analysis is limited to optimizing the single performance objective. When the optimization process involves multiple objectives, Taguchi method may not meet the optimization needs. As such, it is necessary to use a more systematic approach. Fortunately, Taguchi method can be integrated with the Grey Relational Analysis (GRA) to determine the optimal parameter combination [45,47]. As far as the authors' best knowledge, the Taguchi-Grey method has never been used on optimizing the overall on-chip cooling performance of the TFTEC.

In this paper, a framework for the system level optimization of the TFTEC in 3D electronic package system is proposed based on Taguchi-Grey method. Six design factors, including the leg height, the fill-ratio, the electrode height, the gap distance, the hotspot size and the hotspot heat flux have been analyzed. An L_{25} (5^6) orthogonal array is employed to assess the influences of the design factors on the passive and active cooling effects. Furthermore, the optimum design factors for maximizing the cooling effects are approached. This work can provide design guidance for a highly integrated and lightweight chip thermal management system based on the TE cooling.

2. Model description

2.1. Physical model

Fig. 1 illustrates the schematic of 3D electronic package with an integrated TFTEC. Due to the various levels in design factors, Fig. 1 has not been fully drawn to scale for ease of viewing the important structural features. A silicon carbide (SiC) chip with the dimensions of 10 × 10 × 0.4 mm^3 is connected to the integrated heat spreader (IHS) through the thermal interface material (TIM). The TFTEC is embedded in the TIM and is directly attached to the IHS to enhance the heat dissipation capacity [26]. The overall dimensions of the IHS are 30 × 30 × 1.5 mm^3. A dielectric layer is coated between the TFTEC and the IHS, which is neglected because of its ultrathin thickness. An area of hotspot is located at the center of the chip to simulate different hotspot heat flux densities. The TFTEC consists several pairs of TE elements that are assembled electrically in series and thermally in parallel. Each pair of legs consists of a P-type leg and an N-type leg. The footprint of the TFTEC is fixed at 2 × 2 mm^2. The promising Bi_2Te_3/Sb_2Te_3 superlattice materials is employed in this study [8]. The material properties are assumed to be constant due to the narrow operating temperature range. The electrical and thermal parasitic impedances created by the TE material-metal interface and the IHS-TFTEC interface can degrade the intrinsic properties of the TE material and are therefore taken into account. The material properties are presented in Table 1.

Table 1
Material and contact properties [8,48].

Material	Thermal conductivity (W/(m·°C))	Electrical resistivity (Ω·m)	Seebeck coefficient (μV/°C)
TE material	1.2	1.08×10^{-5}	300
SiC	420	–	–
TIM	1.75	–	–
Electrode/lead	398	1.8×10^{-7}	–
Contact interface	Electrical contact resistance (Ω·m^2)	Thermal contact resistance (m^2·°C/W)	
TE material-copper interface	1×10^{-11}	1×10^{-6}	
IHS-TFTEC interface	–	8×10^{-6}	

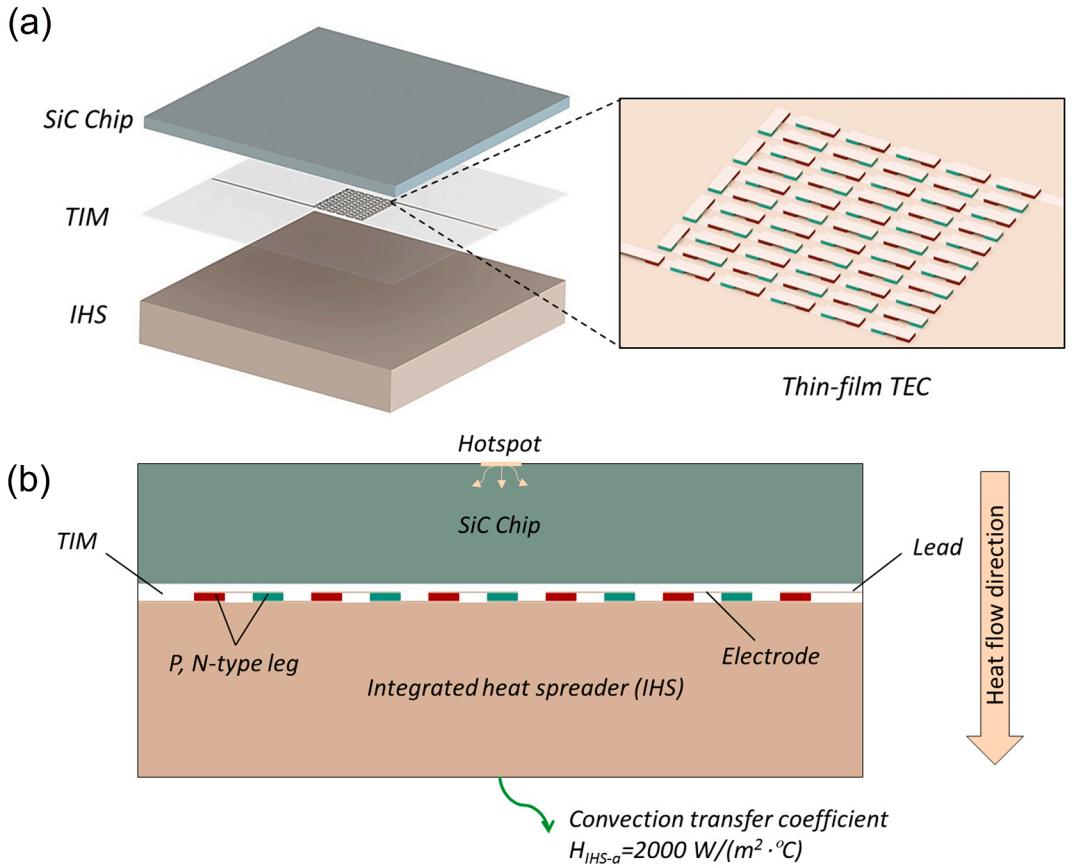


Fig. 1. Schematic of the 3D electronic package with integrated TFTEC: (a) main view and (b) side view.

2.2. Governing equations

The conservation principle of energy and current are expressed as [49]:

$$\vec{\nabla}\cdot\vec{q} = \phi \tag{1}$$

$$\vec{\nabla}\cdot\vec{j} = 0 \tag{2}$$

where q, j and ϕ represent the heat flux vector, steady-state current density and heat generation, respectively.

The steady-state current density $\vec{j}$ is given as [50]:

$$\vec{j} = \frac{1}{\rho}\left(\vec{E} - \alpha\vec{\nabla}T\right) \tag{3}$$

where α, ρ and T represent the Seebeck coefficient, electric resistivity and temperature, respectively. $\vec{E}$ is the electric field vector.

Heat is transported reversibly by the Peltier effect, and is transported irreversibly by the Fourier's law that is affected by the Joule effect. The heat flux vector $\vec{q}$ is given by [50]:

$$\vec{q} = \alpha T\vec{j} - k\vec{\nabla}T \tag{4}$$

where k stands for the thermal conductance.

The heat generation ϕ can be expressed as:

$$\phi = \vec{E}\cdot\vec{j} = j^2\rho + \vec{j}\cdot\alpha\vec{\nabla}T \tag{5}$$

The steady-state thermal energy transport equation that couples temperature and electrical current density is given by [50]:

$$\nabla(k\vec{\nabla}T) + \rho\vec{j}^2 - T\vec{j}\cdot\left[\left(\frac{\partial\alpha}{\partial T}\right)\vec{\nabla}T + (\nabla\alpha)_T\right] = 0 \tag{6}$$

The cooling power Q_c can be used to analyze the performance of the TFTEC, which is given by.

$$Q_c = \alpha T_{cm} I_m - \frac{1}{2}I^2R - k(T_{hm} - T_{cm}) \tag{7}$$

where I is the current, T_{cm} is the mean temperature at the cold end, T_{hm} is the mean temperature at the hot end. R is the electrical resistance, and k is the thermal conductance, which are given by.

$$k = \frac{k_n A_n}{l_n} + \frac{k_p A_p}{l_p} \tag{8}$$

$$R = \frac{\rho_n l_n}{A_n} + \frac{\rho_p l_p}{A_p} \tag{9}$$

The passive cooling effect (ΔT_{pas}) and the active cooling effect (ΔT_{act}) can be calculated by.

$$\Delta T_{pas} = T_{hs}(0) - T_{hs}(1) \tag{10}$$

$$\Delta T_{act} = T_{hs}(1) - T_{hs}(2) \tag{11}$$

where T_{hs} (0) is the maximum temperature of the chip hotspot without integrated TFTEC. T_{hs} (1) is the maximum temperature of the chip hotspot when the TFTEC is integrated, but no current is introduced. T_{hs} (2) is the maximum temperature of the chip hotspot when the TFTEC is integrated under the optimal current condition.

2.3. Numerical method

To avoid the interference of unimportant factors, we have introduced some reasonable assumptions:

(1) All surfaces except the IHS-ambient and chip surfaces in the electronic package are insulated.
(2) All materials in the package are isotropic.
(3) The effect of heat radiation is neglected.

The IHS-ambient surface is set to fixed convection condition, with a heat transfer coefficient of 2000 W/(m^2•°C) [25,40]. The heat flux of hotspot area is set to q_{hs} = 500–3000 W/cm^2 to simulate different hotspot heat flux densities. The remaining part of the chip keeps a background heat flux of 50 W/cm^2. One end of the TFTEC lead is grounded, and the other end is applied with an optimal current. The boundary conditions used in the numerical simulations are shown in Table 2.

The 3D numerical simulations are performed using the commercial software ANSYS Workbench platform. The iterations continue until the relative error of each variable is lower than 1×10^{-4}. The combination of A1, B1, C1, D1, E1 and F1 is used as a typical structure for grid independence test because of its smallest structure size and complex grid system. Three different grid systems with total elements of 213,571, 350,194 and 471,295 are tested. When the TFTEC is not powered, the simulation results show that the hotspot temperatures are 70.43 °C, 70.38 °C, and 70.39 °C, respectively. When a current of 0.1 A is introduced, the chip hotspot temperatures are 70.12 °C, 70.09 °C, and 70.12 °C, respectively. The hotspot temperature in different grid systems are changed less than 1%. Therefore, the numerical results used in the model are grid-independent.

2.4. Model validation

Experiments have been performed to validate the numerical model. The experimental setup consists of a ceramic heater, a miniature TEC module, a thermal pad and a heat spreader. The ceramic heater with dimensions of 10 × 10 × 1.5 mm^3 is used to continuously heat up the cold side of the miniature TEC module. A programmable direct current (DC) power supply (PDS 2200-50F) is used to control the heating power of the ceramic heater, with the range of output DC voltage is 0–200 V and the range of output DC current is 0–50 A. The miniature TEC module with dimensions of 4 × 4 × 0.8 mm^3 (30 pairs of thermocouples) is embedded in the thermal pad. The thermal pad with dimensions of 10 × 10 × 1 mm^3 is easy to use and is suitable for chip cooling test. The miniature TEC module is powered by lab DC power supply (Keysight E3634A), with the range of output DC voltage is 0–50 V and the range of output DC current is 0–7 A. The hot side of the TEC is connected to the heat spreader with dimensions of 30 × 30 × 1.5 mm^3. The experimental setup is placed in a natural convection air environment. A portable infrared camera from FLIR T650sc (with an accuracy of ± 1%) is used to capture the maximum temperature change of the ceramic heater. Fig. 2 (a) presents the infrared image when the ceramic heater and miniature TEC module are both powered. Fig. 2(b) shows the comparisons between the numerical results with the experimental results under fixed heating powers. It can be seen that the simulations match well with the experimental results. The discrepancy may result from the temperature dependent material properties and environmental noise in the experiments, which are neglected in the simulation model. Nonetheless, the maximum error is within 4%, thus the numerical model is feasible.

2.5. Optimization method

2.5.1. The principle of the Taguchi method

The signal-to-noise (S/N) ratio is employed to evaluate the sensi-

Table 2
Boundary conditions.

Surface	Boundary type	Value
IHS-ambient	Convection	$H_{IHS\text{-}a}$ = 2000 W/(m^2•°C)
Hotspot area	Heat flux	q_{hs} = 500–3000 W/cm^2
Chip non-hotspot area	Heat flux	q_b = 50 W/cm^2
One end of the TFTEC lead	Voltage	V = 0 V
One end of the TFTEC lead	Current	I = 0–4.6 A

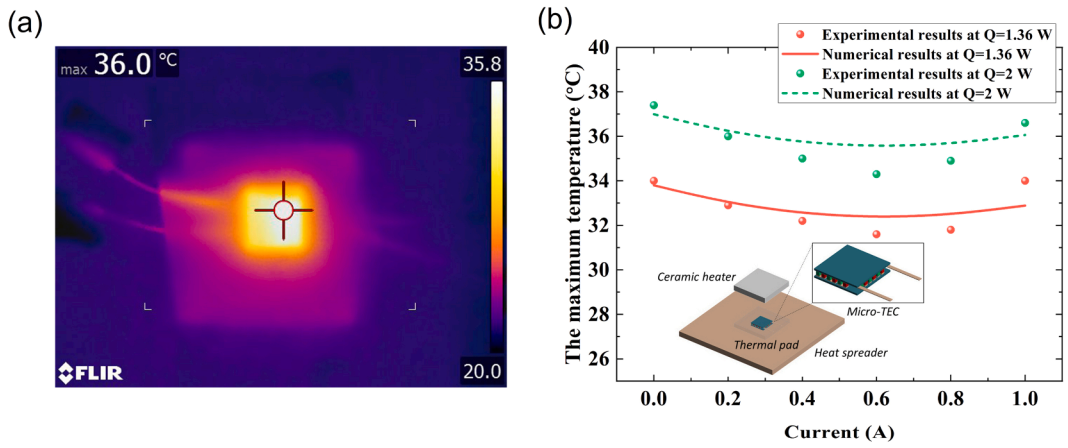


Fig. 2. Experimental results: (a) Infrared image and (b) comparisons between the numerical results with the experimental results.

tivity of the design factors on the cooling performance of the TFTEC. There are three categories of S/N ratio, including "Larger is better", "Smaller is better" and "Nominal is better". Since the objective of the study is to achieve better cooling performance, it is expected that passive cooling and active cooling can achieve the maximum values. Therefore, "Larger is better" is thus used for passive cooling and active cooling.

$$\text{Larger is better} S/N(dB) = -10\log_{10}\left[\frac{1}{R}\sum_{i=1}^{R}\frac{1}{y_i^2}\right] \tag{12}$$

where R is the number of repetitions in each simulation, and y_i represents the value of the passive cooling or active cooling for the ith trial. The factor level with the highest S/N ratio is called the optimal level.

The commercial program Minitab 19 is employed to analyze the S/N ratios. The chip heat load has been confirmed in our previous research [48] to affect the cooling performance of TFTEC. Six key factors that influence the cooling performance of the TFTEC are evaluated, namely, the leg height (A), the fill ratio (B), the electrode height (C), the gap distance (D), the hotspot size (E) and the hotspot heat flux (F). Each design factor is evaluated at five different levels. The selected factors and levels are shown in Table 3.

2.5.2. Analysis of variance

After the S/N ratio analysis is completed, the analysis of variance (ANOVA) is conducted to analyze the mean S/N ratio under each factor level to determine the contribution ratio of each factor on the performance of the TFTEC. The ANOVA includes degrees of freedom (DOF), sum of squares (SS), variance (V) and the percentage contribution of each factor. For factor i, degree of freedom $(DOF)_i$, sum of squares $(SS)_i$, variance V_i and contribution P_i are calculated as follows:

$$(DOF)_i = k_i - 1 \tag{13}$$

$$(SS)_i = \sum_{j=1}^{k_i}\frac{S_{ij}^2}{k_i} - S_m \tag{14}$$

$$V_i = \frac{(SS)_i}{(DOF)_i} \tag{15}$$

$$P_i = \frac{(SS)_i}{(SS)_T} \tag{16}$$

where k_i is the number of levels of factor i, S_{ij} is the sum of the S/N ratios of factor i in level j, and S_m is the correction factor, which is calculated as:

$$S_m = \frac{1}{n}\left(\sum_{i=1}^{n}(S/N)_i\right)^2 \tag{17}$$

where n represents the total number of simulations, and $(SS)_T$ is called the sum of squares, can be given by:

$$(SS)_T = \sum_{i=1}^{n}(S/N)_i^2 - S_m \tag{18}$$

2.5.3. Grey relational analysis

Taguchi analysis can be integrated with the GRA to optimize multiple performance indicators simultaneously. GRA utilizes grey system theory to identify complicated relationships when there are multiple objectives. The level of similarity and variability of design factors are fundamental parts of GRA [51]. The calculation steps of the GRA have been developed for this purpose can be executed as follows:

First, each objective is normalized to make it dimensionless and avoid variability. Depending on whether the objective is needed to be maximized or minimized, the value of each objective is normalized between 0 and 1. There are three criterions for normalization in the analysis, including "Larger is better", "Smaller is better" and "Nominal is better". The criterion "larger is better" is used for passive cooling and

Table 3
Selected factors and levels for Taguchi method optimization.

Label	Factor	Notation	Level				
			1	2	3	4	5
A	Leg height	h_{TE} (μm)	5	10	15	20	25
B	Fill ratio	r_{fill}	0.16 (256 legs)	0.3025 (121 legs)	0.49 (49 legs)	0.5625 (25 legs)	0.64 (9 legs)
C	Electrode height	h_E (μm)	5	10	20	30	40
D	Gap distance	d_{gap} (μm)	5	10	15	20	25
E	Hotspot size	A_{hs} (μm^2)	200 × 200	400 × 400	600 × 600	800 × 800	1000 × 1000
F	Hotspot heat flux	q_{hs} (W/cm^2)	500	1000	1500	2000	3000

active cooling, as shown in Eq. (34). The normalized value of the objective of all tests in the orthogonal array is termed as the reference sequence [47,52].

$$\text{Larger is better} x_i^*(k) = \frac{x_i^0(k) - \max x_i^0(k)}{\max x_i^0(k) - \min x_i^0(k)} \tag{19}$$

where, $x_i^*(k)$ is the normalized value of the k^{th} objective in the i^{th} sequence. $x_i^0(k)$ is the objective in the i^{th} sequence. $\max x_i^0(k)$ is the maximum value of $x_i^0(k)$. $\min x_i^0(k)$ is the minimum value of $x_i^0(k)$.

The deviation sequence is defined from the data of reference sequence [45,52]:

$$\Delta_i = \left\| \max x_i^*(k) - x_i^*(k) \right\| \tag{20}$$

where, Δ_i is the deviation sequence, $\max x_i^*(k)$ is the maximum value of reference sequence.

Then, the Gray Relational Coefficient (GRC) can be evaluated by the deviation sequence, the expression can be given as [45,52]:

$$\xi_i(k) = \frac{\Delta_{\min} + \psi \Delta_{\max}}{\Delta_i(k) + \psi \Delta_{\max}} \tag{21}$$

where, $\xi_i(k)$ is the GRC. $\Delta_{\max}$ and $\Delta_{\min}$ are the maximum and minimum values of deviation sequences, respectively. ψ is the distinguishing or identification coefficient, its value lies in the interval [0,1], and the commonly used value is 0.5 [52,53].

Finally, the GRCs of the multiple quality objectives of each orthogonal array are used to calculate the Grey Relational Grade (GRG) of the array. The general equation for evaluating GRG using the value of the GRC is shown by [52,53]:

$$\gamma_i = \frac{1}{\sum_{k=1}^{n} w_k} \sum_{k=1}^{n} w_k \xi_i(k) \tag{22}$$

where, γ_i is the GRG for i^{th} experiment, w_k is the normalized weight value of k^{th} objective. Since active cooling is generally regarded as a distinctive indicator for evaluating TFTEC performance, the weightages for identifying the optimum design parameters are arbitrarily divided as follows: passive cooling is 0.4 and active cooling is 0.6. All combinations

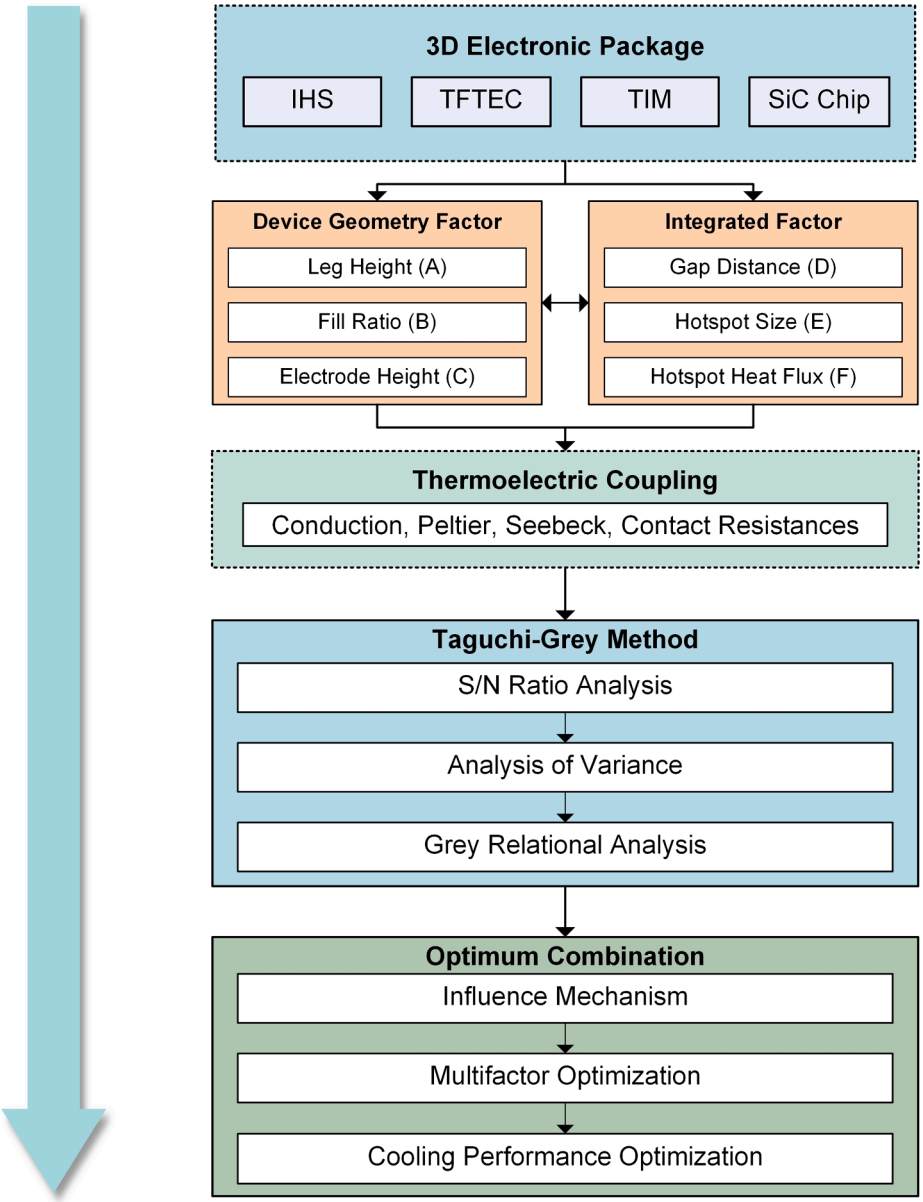


Fig. 3. Integrated design flow of the 3D electronic package with an integrated TFTEC.

of the orthogonal sequence are sorted by GRG value. The combination with the maximum GRG value is ranked 1, the combination with the minimum GRG value is rank 25. Thus, the combination with the maximum GRG is recommended as the potential optimum combination. For better visualization, the integrated design flow of the 3D electronic package with an embedded TFTEC is presented in Fig. 3.

3. Results and analysis

3.1. Factorial analysis

Table 4 shows the computational values of 25 Runs in the L_{25} orthogonal array. The maximum passive cooling of 15.92 °C is exhibited at Run 5, whereas the minimum passive cooling of 3.631 °C is appeared at Run 15. This pronounced difference between the maximum passive cooling and the minimum one indicates that these design factors with appropriate levels play an important role on the passive cooling performance of the TFTEC. Moreover, since the TFTEC contains a large number of highly conductive metal electrodes, its effective thermal conductivity exceeds the thermal conductivity of TIM (1.75 W/(m·°C)). The integration of TFTEC in the TIM shows a remarkable passive cooling effect. It should also be noted that the magnitude of passive cooling is related to the thermal conductivity of the TIM used. For active cooling, the maximum value of 4.487 °C is presented at Run 13, while the minimum value of 0.186 °C is appeared at Run 10. The passive cooling dominated by Fourier effect is appeared to be more dominant. As a result, these two objectives have different effects on the design factors, making it impossible to find the optimal combination of design factors in a single run.

The mean responses of S/N ratios in terms of passive cooling and active cooling at each level of six factors are listed in Table 5 and Table 6. As a result, the influence of the six factors on passive cooling is ranked as: $h_E > A_{hs} > q_{hs} > h_{TE} > d_{gap} > r_{fill}$. For active cooling, the influence of the six factors is ranked as: $h_E > h_{TE} > d_{gap} > r_{fill} > A_{hs} > q_{hs}$. In light of the mean S/N ratio is changed with each level, Fig. 4 plots the profiles of mean S/N ratios for better visualization.

Table 4
Results of numerical simulation in L_{25} (5^6) orthogonal array.

Run	A h_{TE} (μm)	B r_{fill}	C h_E (μm)	D d_{gap} (μm)	E A_{hs} (μm^2)	F q_{hs} (W/cm^2)	ΔT_{pas} (°C)	ΔT_{act} (°C)
1	1	1	1	1	1	1	3.995	0.335
2	1	2	2	2	2	2	4.793	0.529
3	1	3	3	3	3	3	6.755	0.689
4	1	4	4	4	4	4	9.73	0.68
5	1	5	5	5	5	5	15.92	0.77
6	2	1	2	3	4	5	7.33	0.98
7	2	2	3	4	5	1	5.814	1.437
8	2	3	4	5	1	2	5.839	1.611
9	2	4	5	1	2	3	9.119	3.128
10	2	5	1	2	3	4	4.473	0.186
11	3	1	3	5	2	4	5.27	1.27
12	3	2	4	1	3	5	8.85	4.36
13	3	3	5	2	4	1	8.094	4.487
14	3	4	1	3	5	2	4.73	0.38
15	3	5	2	4	1	3	3.631	0.502
16	4	1	4	2	5	3	8.43	2.86
17	4	2	5	3	1	4	6.513	3.863
18	4	3	1	4	2	5	4.31	0.74
19	4	4	2	5	3	1	3.922	0.834
20	4	5	3	1	4	2	5.73	2.214
21	5	1	5	4	3	2	6.68	2.45
22	5	2	1	5	4	3	4.91	1.12
23	5	3	2	1	5	4	6.72	2.83
24	5	4	3	2	1	5	4.381	2.634
25	5	5	4	3	2	1	5.072	2.952

Table 5
Response table for S/N ratios in terms of passive cooling.

Level	A	B	C	D	E	F
	h_{TE} (μm)	r_{fill}	h_E (μm)	d_{gap} (μm)	A_{hs} (μm^2)	q_{hs} (W/cm^2)
1	17.21	15.76	13.01	16.38	13.53	14.29
2	16.03	15.59	14.11	15.23	14.81	14.82
3	15.25	15.86	14.86	15.55	15.38	15.87
4	14.90	15.43	17.33	15.09	16.84	16.01
5	14.76	15.50	18.83	15.90	17.58	17.16
Delta	2.45	0.43	5.82	1.29	4.04	2.87
Rank	4	6	1	5	2	3

Table 6
Response table for S/N ratios in terms of active cooling.

Level	A	B	C	D	E	F
	h_{TE} (μm)	r_{fill}	h_E (μm)	d_{gap} (μm)	A_{hs} (μm^2)	q_{hs} (W/cm^2)
1	−4.7771	1.8624	−6.8288	5.8270	1.7615	2.9030
2	0.4822	4.6262	−0.8466	2.0876	2.6475	0.9787
3	2.7029	4.0732	3.4611	1.8651	0.2302	2.1591
4	4.7155	0.9974	6.4223	−0.2037	3.4803	0.9781
5	7.1236	−1.3120	8.0392	0.6711	2.1275	3.2282
Delta	11.9007	5.9382	14.8681	6.0308	3.2501	2.2501
Rank	2	4	1	3	5	6

(1) Leg height (h_{TE})

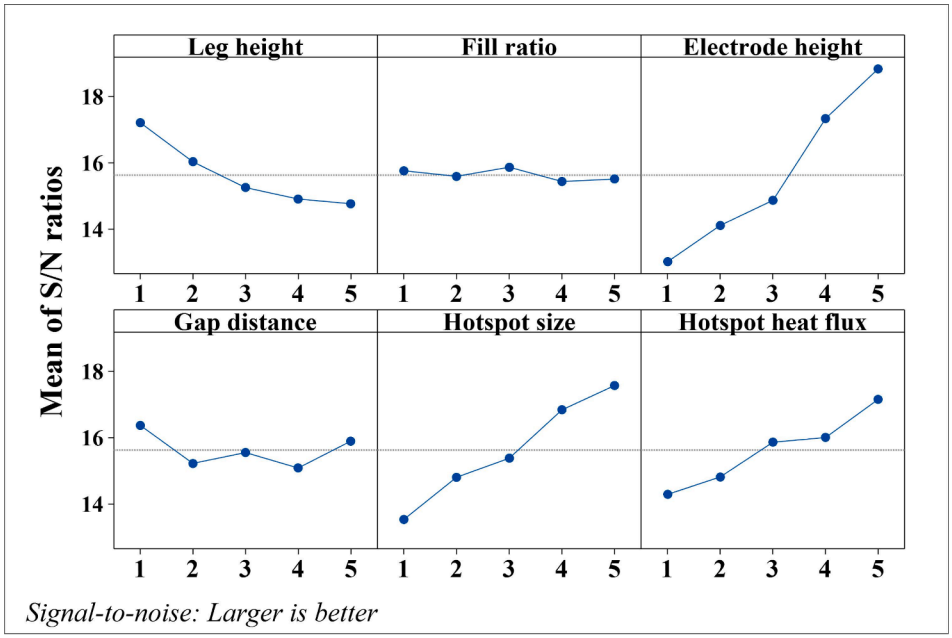
As the TE leg height is increased from 5 μm to 25 μm, the passive cooling of the TFTEC is continued to decrease, whereas the active cooling is increased. Refer to Eqs. (8)-(9), increasing the leg height would lead to larger device thermal resistance and larger device electrical resistance. Larger thermal resistance would reduce the passive cooling, but it would also enhance the Peltier active cooling effect by reducing the Fourier loss. Larger electrical resistance would lead to more Joule heat loss, which is a negative effect on the active cooling of the TFTEC. In the present study, it shows that the increase in leg height has a limited effect on the electrical resistance, but it can greatly reduce the Fourier heat conduction, thereby enhancing active cooling. As a result, with the increase of the leg height, there is a trade-off between the mean S/N ratios of the passive cooling and that of the active cooling. The TE leg height can be regarded as a key factor that determines these two different cooling modes of passive cooling and active cooling.

(2) Fill ratio (r_{fill})

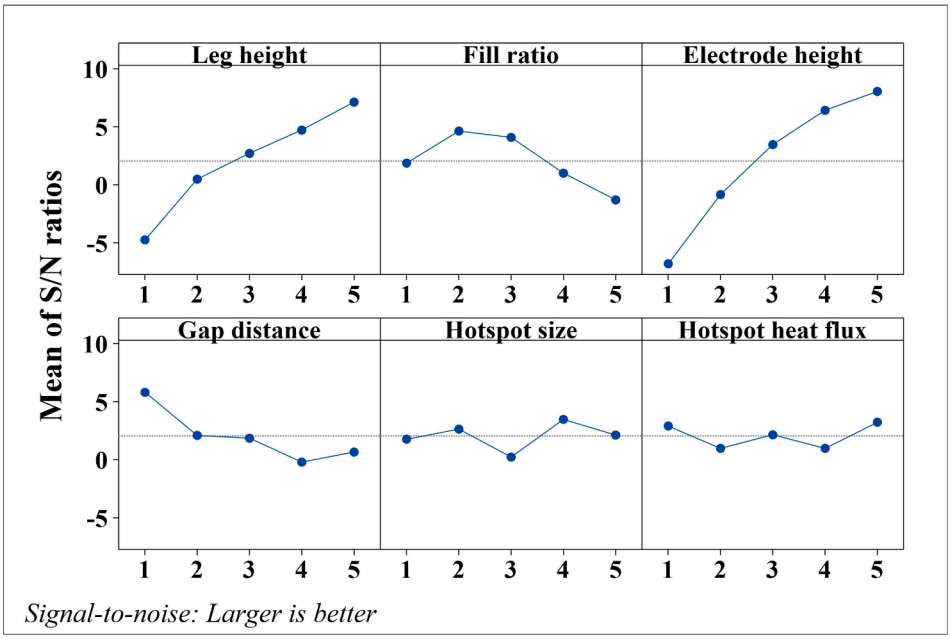
Within a given footprint, the variation of the fill ratio would not only change the number of legs, but also change the cross-sectional area of the leg. In the present study, when the fill ratio is increased, the number of legs decreases, whereas the cross-sectional area of the leg is increased. The increase in the number of legs is proven to be beneficial to improve the cooling performance of TEC [49]. Refer to Eqs. (8) and (9), larger cross-sectional area of the leg also can reduce the electrical and thermal resistances of the leg. Therefore, there is an optimal fill ratio to optimize the cooling performance. It can be seen from Fig. 4(a) that when the fill ratio is at level 3, passive cooling can achieve the maximum value. For the maximum active cooling, the fill ratio is preferred at level 2, as shown in Fig. 4(b).

(3) Electrode height (h_E)

As shown in Fig. 4, when the electrode height is increased, the passive and active cooling effects of the TFTEC are enhanced rapidly. Thus, for the two cooling effects, level 5 is preferred. One reason is that the increase in electrode height increases the proportion of metals with high thermal conductivity in the TFTEC, which is leaded to an increase in the effective thermal conductivity of the device. In refrigeration, lower



(a) Passive cooling



(b) Active cooling

Fig. 4. Profiles of mean S/N ratios.

device effective thermal conductivity reduces the backflow of Fourier heat from the hot side (IHS) to the cold side (chip heat source) and is therefore preferred. However, when the TFTEC is integrated for on-chip cooling, the Peltier heat flows from the hot side to the cold side, augmenting Fourier heat conduction, rather than opposing it. One other point, the increase of the electrode height is beneficial to reduce the electrical resistance of the device. As a result, increasing the electrode height is beneficial to improve the cooling effects of the TFTEC.

(4) Gap distance (d_{gap})

The gap distance is the distance between the chip and the TFTEC in the TIM, which also is the additional thermal resistance on the cold end of the TFTEC. The heat generated by the chip should pass through the gap distance and then arrive at the cold end of the TFTEC. As shown in Fig. 4, it can be seen that a minimized (5 μm in this study) gap distance is conductive to the cooling effects of the TFTEC. Thus, level 1 is preferred for both cooling effects.

(5) Hotspot size (A_{hs})

When the hotspot heat flux is constant, the change in the hotspot size would directly affect the amount of generated heat. The larger the hotspot size, the higher the hotspot temperature. Since the passive effect

is driven by the temperature gradient, the change of the hotspot temperature would also affect the passive cooling of the TFTEC. Moreover, the hotspot heat flux would also affect the net heat absorption of the cold junction of the TFTEC. However, the influence of chip heat flow on active cooling is more reflected in Fourier heat conduction, and even this influence is positive. Therefore, passive cooling is more sensitive to the hotspot size than active cooling. As the hotspot size is increased, the passive cooling effect can be greatly improved.

(6) Hotspot heat flux (q_{hs})

At a fixed hotspot size, the change of hotspot heat flux would also determine the amount of heat generation and the hotspot temperature. With the increase of hotspot heat flux, the passive cooling effect is enhanced, while the trend of active cooling is presented as disorderly. When the hotspot heat flux is 3000 W/cm^2, i.e., at level 5, the maximum passive and active cooling effects can be achieved. In addition, it can be seen that when the hotspot heat flux is increased from 500 W/cm^2 to 3000 W/cm^2, the TFTEC still has excellent hotspot removal ability.

The contribution ratios of design factors are plotted in Fig. 5, calculated by the contribution of each factor to the overall response. As shown, the electrode height is the most important design factor that affects the passive cooling and active cooling, contributing for 45.5% and 45.3%, respectively. For passive cooling, the hotspot size, hotspot heat flux and leg height account for relatively large proportions, which are 21.4%, 14.7% and 13.7%, respectively. The other two factors play insignificant roles on the passive cooling effect, contributing only 4.7% in total. In terms of active cooling, leg height and gap distance also contribute a lot, with 25.7% and 18.8% respectively. Meanwhile, the fill ratio contributes 7.5%. However, the hotspot parameters have little influence on the active cooling effect, accounting for only about 2.7% in total. These quantitative results can give a full picture of the influence mechanism of the design factors for the TFTEC.

3.2. Multifactor optimization

Based on the above analysis, it can be clearly shown that it is easy to use S/N ratio analysis and ANOVA to individually evaluate the influence of design factors on each objective. However, when multiple objectives are involved in the optimization process, no single design factor could meet all required objectives. Therefore, it is necessary to use a more systematic method, such as GRA, to derive the optimum design factors by using a weighting method to compromise each objective. Using Eqs. (19)-(22) to normalize the data in Table 4, the normalized objectives can be obtained, as shown in Table 7. The combination with the maximum GRG value ranks 1 and the combination with the minimum GRG value ranks 25. As shown, the maximum experiment of GRG is Run 13, which can be considered as the potential optimum combination.

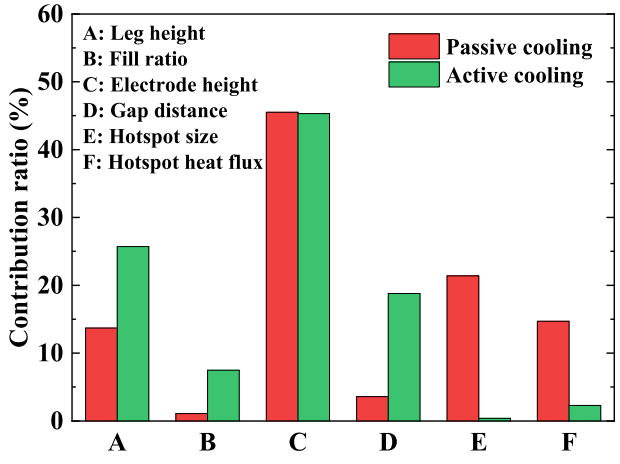


Fig. 5. Factor contribution ratios.

Table 7
Normalized response, grey relational coefficients and grey relational grade for the TFTEC.

Run	Normalized response		GRC		GRG	Orders
	Passive cooling	Active cooling	Passive cooling	Active cooling		
1	0.030	0.035	0.340	0.341	0.341	2
2	0.095	0.080	0.356	0.352	0.354	5
3	0.254	0.117	0.401	0.362	0.377	8
4	0.496	0.115	0.498	0.361	0.416	14
5	1.000	0.136	1.000	0.367	0.620	22
6	0.301	0.185	0.417	0.380	0.395	11
7	0.178	0.291	0.378	0.414	0.399	12
8	0.180	0.331	0.379	0.428	0.408	13
9	0.447	0.684	0.475	0.613	0.558	21
10	0.069	0.000	0.349	0.333	0.340	1
11	0.133	0.252	0.366	0.401	0.387	10
12	0.425	0.970	0.465	0.944	0.753	24
13	0.363	1.000	0.440	1.000	0.776	25
14	0.089	0.045	0.354	0.344	0.348	4
15	0.000	0.073	0.333	0.351	0.344	3
16	0.391	0.622	0.451	0.569	0.522	20
17	0.235	0.855	0.395	0.775	0.623	23
18	0.055	0.129	0.346	0.365	0.357	6
19	0.024	0.151	0.339	0.371	0.358	7
20	0.171	0.472	0.376	0.486	0.442	15
21	0.248	0.526	0.399	0.514	0.468	17
22	0.104	0.217	0.358	0.390	0.377	9
23	0.251	0.615	0.400	0.565	0.499	19
24	0.061	0.569	0.347	0.537	0.461	16
25	0.117	0.643	0.362	0.584	0.495	18

Fig. 6 shows the average GRG response graph drawn according to the L_{25} orthogonal array. As shown, the most ideal candidates for the optimum design factor are the leg height (A) at level 3 (15 μm), the fill ratio (B) at level 2 (0.3025), the electrode height (C) at level 5 (40 μm), the gap distance (D) at level 1 (5 μm), the hotspot size (E) at level 5 (1000 × 1000 μm^2), and the hotspot heat flux at level 5 (3000 W/cm^2). Therefore, according to the average GRG response graph, the optimal design combination of the TFTEC should be A3, B2, C5, D1, E5 and F5. By comparing the orthogonal array in Table 4 with the curve in Fig. 6, it is found that the simulation corresponding to the optimal design factor combination has not been performed. Therefore, it is necessary to confirm and verify these potential optimal design factor combinations.

3.3. Verification of the optimum combination of design factors

It is known from Table 4 that Run 5 has the largest passive cooling effect. Run 13 has the maximum active cooling. Based on S/N ratio analysis and ANOVA, the combination of design factors for maximizing the passive cooling of the TFTEC should be A1, B3, C5, D1, E5 and F5. For maximizing the active cooling effect, it can be seen that the optimum combination should be A5, B2, C5, D1, E4 and F5. Furthermore, according to GRA, Run 13 and A3, B2, C5, D1, E5 and F5 are also potentially the optimum combination of design factors. Therefore, to ascertain the optimum combination, five cases listed in Table 8 are tested and compared with each other.

Fig. 7 compares the hotspot cooling performance of TFTEC in five cases. It can be found that the passive cooling of Case 1 obtained from the orthogonal array reaches 15.92 °C, but its active cooling is only 0.77 °C. Case 2 is the combination with the maximum active cooling performance in the orthogonal array, but it is also only 4.49 °C. At the same time its passive cooling reduces by 3.83 °C compared to Case 1. Both Case 3 and Case 4 are obtained by S/N ratio analysis and ANOVA. Among them, the passive cooling of Case 3 reaches 23.28 °C, but its active cooling was only a measly 2.89 °C. The active cooling of Case 4 has broken through to 10.96 °C, but its passive cooling has also

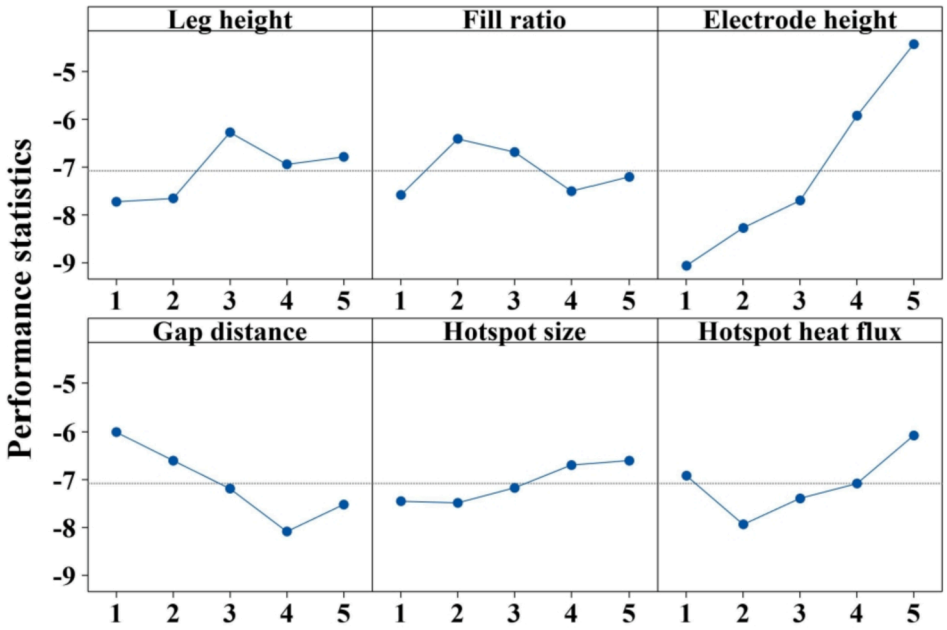


Fig. 6. Average Grey relational grades for combination of all objectives.

Table 8
Level combinations for the TFTEC comparisons.

Case	Level					
	Factor A	Factor B	Factor C	Factor D	Factor E	Factor F
	h_{TE} (μm)	r_{fill}	h_E (μm)	d_{gap} (μm)	A_{hs} (μm^2)	q_{hs} (W/cm^2)
1	1	5	5	5	5	5
2	3	3	5	2	4	1
3	1	3	5	1	5	5
4	5	2	5	1	4	5
5	3	2	5	1	5	5

experienced a significant reduction, leaving only 10.82 °C. This proves that there is indeed a trade-off between passive cooling and active cooling. After compromise and optimization by GRA, Case 5 shows a more superior active cooling performance, reaching 12.29 °C. Although the passive cooling of Case 5 is 6.46 °C lower than that of Case 3, it can achieve a total cooling of 29.11 °C due to its substantial enhancement in active cooling performance. The total cooling for Case 3 and Case 4 is only 26.17 °C and 21.78 °C, respectively. As a result, the combination of Case 5 obtained using the Taguchi-Grey method is verified to be the optimal combination, with a passive cooling of 16.82 °C and an active cooling of 12.29 °C.

Since electrode height and leg height have a decisive influence on active cooling, Fig. 8 plots the effects of electrode height and leg height on cooling performance based on the Case 5. As the electrode height increases, the effective thermal conductivity of the device increases, and the TIM thickness also increases gradually. The heat generated by the chip is more transferred outward through the TFTEC, which enables its passive cooling to be significantly improved. However, when the electrode height is small and the current is large, it can be found that the active cooling shows a negative value, reaching about −50 °C, which can be called "negative temperature region" (NTR). This region appears mainly because the TFTEC loses its cooling effect and completely becomes a resistive heater, which generates a lot of Joule heat and increases the chip hotspot temperature. With the increase of the electrode height, the thermal resistance of the device is reduced, and the accumulated Joule heat is also alleviated, so that the active cooling of the TFTEC rises and finally reaches 12.4 °C. Hence, increasing the electrode height is beneficial to move away from the NTR and simultaneously improve passive and active cooling.

With the increasing leg height, TIM thickness gradually increases, but passive cooling decreases gradually. This can be attributed to the poor thermal conductivity (1.2 W/(m·°C)) of TE materials. The increase in the leg height further increases the device thermal resistance, resulting in a significant decrease in passive cooling. On the other hand, the active cooling of TFTEC shows a slightly enhanced trend with the increasing leg height, reaching a maximum of 12.6 °C. However, when the TE leg height is large (>15 μm), the device electrical resistance is increased due to the high electrical resistivity of the TE material (1.08×10^{-5} Ω·m). If the input current of the TFTEC is large (4 A), a large amount of Joule heat will be generated, causing the device to lose cooling performance, and eventually the NTR will appear. Therefore, increasing the leg height is not entirely beneficial, especially as it increases the thermal and electrical resistances of the device.

3.4. Power consumption analysis

Fig. 9 visually shows the effect of TFTEC on power devices in terms of power consumption. Four kinds of power devices were selected, including SiC MOSFET C3M0120100K (Case 1) [54], SiC MOSFET C2M0025120D (Case 2)[55], SiC MOSFET module WAS300M12BM2 (Case 3) [56] and HiPak IGBT module 5SNG 0250P330305 (Case 4) [57]. According to the power consumption data and thermal resistance data of the power devices and modules in the datasheet, the temperature drop of the chip hotspot can be roughly converted into the power consumption change. For low-power discrete devices, passive cooling can reduce the chip power consumption by about 11 W, and active cooling can further reduce it by 8 W. As the power consumption of the power device increases, its power consumption reduction effect is augmented. For the HiPak IGBT module, the power consumption reaches an astonishing 2450 W. After integrating the TFTEC, its passive cooling effect reduces its power consumption by 329 W when the TFTEC is not powered. When the TFTEC is powered on, its power consumption continues to be reduced by 241 W by exerting a TE cooling effect. Thus, TFTEC enables a considerable reduction in chip power consumption in power devices that was limited by chip temperature. Besides, referring to the 10 °C junction temperature law [58] commonly used in power devices, TFTEC-based on-chip thermal management also has long-term

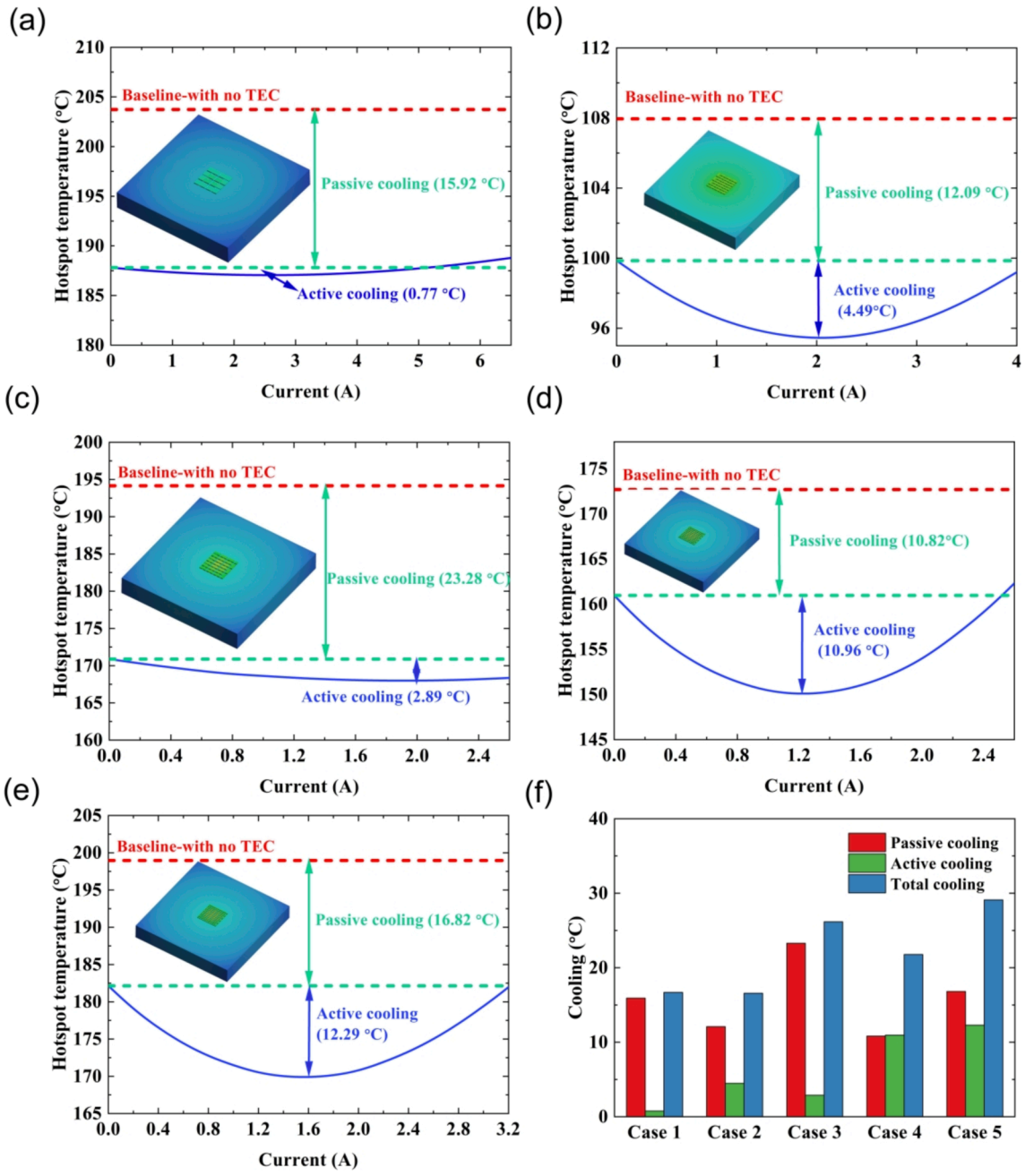


Fig. 7. Hotspot cooling performance: (a) Case 1; (b) Case 2; (c) Case 3; (d) Case 4; (e) Case 5 and (f) comparisons.

reliability benefits. However, such excellent TE cooling performance comes at cost of the TFTEC power consumption. The power consumption of the TFTEC under the optimal current condition is only about 7 W, which corresponds to only 8% of the power consumption of Case 1 and 3% of the power consumption of Case 4.

4. Discussion

In the present study, we propose a system-level optimization framework for TFTEC in 3D integration based on Taguchi-Grey method. The cooling performance of the TFTEC can be maximized based on the electrode-height-priority principle and the optimal leg height as well as the optimal fill ratio. These structural factors are also easily realized based on semiconductor micro-nano processes, such as electrode height and leg height can be achieved using chemical vapor deposition, physical vapor deposition and electrochemical deposition processes. For example, for thick TE legs that are difficult to fabricate, Chowdhury et al. [8] fabricated a thin (~100 μm total thickness) TFTEC made of ultrathin (5 ~ 8 μm thick) nanostructured Bi_2Te_3-based thin-film superlattice material by MOCVD method. Shen et al. [59,60] fabricated p-type Sb_2Te_3 and n-type Bi_2Te_3 films of different thicknesses using physical vapor deposition method. The thickness of p-type Sb_2Te_3 film reached 16 μm, and the thickness of n-type Bi_2Te_3 film reached 18 μm. Snyder et al. [61] fabricated a TFTEC containing 126n-type and p-type $(Bi,Sb)_2Te_3$ TE elements (60 μm in diameter and 20 μm tall) by the ECD method. As such, the superlattice-based TFTEC can achieve a cooling capacity of up to 29.11 °C for the target local hotspot (1000 × 1000 μm^2) with a heat flux density of 3000 W/cm^2. Thereinto, passive cooling contributes 16.82 °C and active cooling contributes 12.29 °C. This integrated design framework offers the possibility of efficient TE cooling of 3D integrated high power density electronic devices that are no longer limited by local high heat flux density.

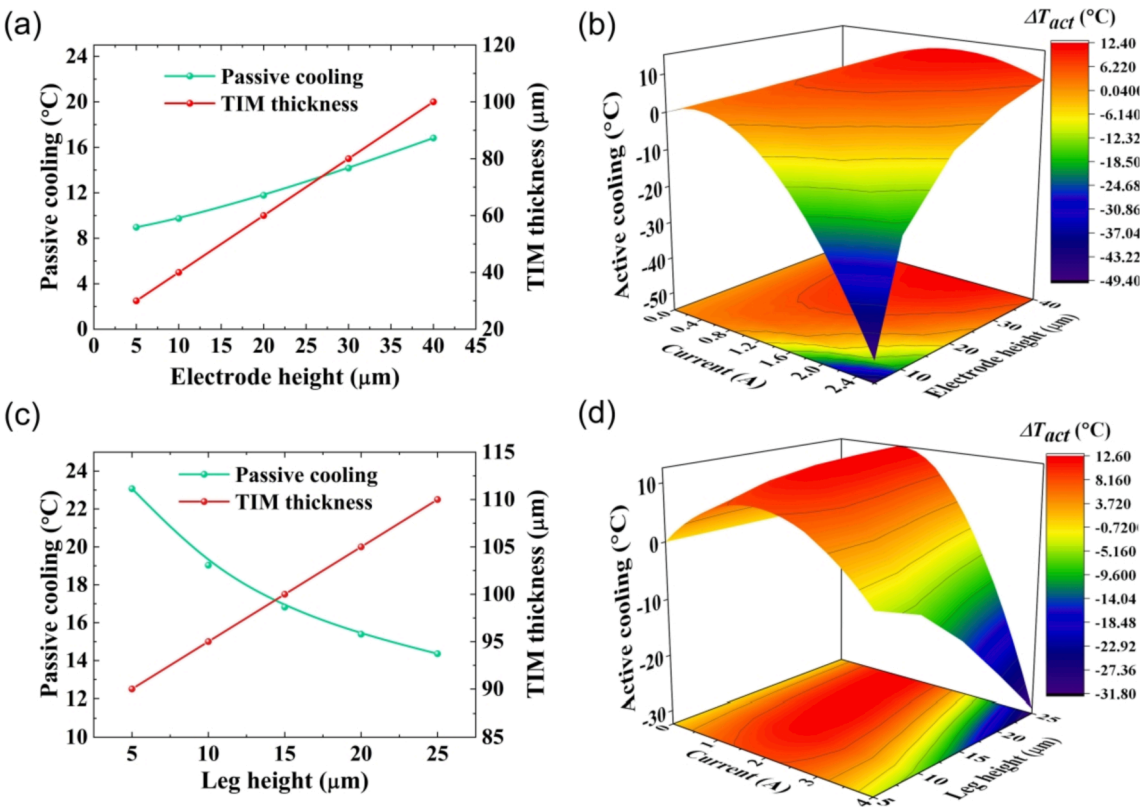


Fig. 8. Verification of the effects of electrode height and leg height on cooling performance: (a) the effect of electrode height on passive cooling; (b) the effect of electrode height on active cooling (c) the effect of leg height on passive cooling and (d) the effect of leg height on active cooling.

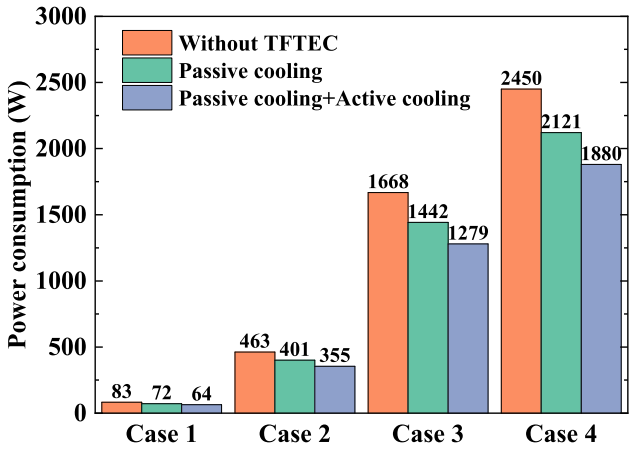


Fig. 9. Power consumption comparison.

It is worth noting that since the chip hotspot temperature in this study is up to 200 °C, both passive cooling and active cooling are higher than the reported values in the Refs. [8,26]. Higher chip hotspot temperatures will significantly enhance the passive cooling effect and slightly promote the active cooling effect, which has also been reported in the Ref. [26]. Actually, high-temperature operating points of 200–250 °C [2] are common in third-generation wide-bandgap semiconductor devices. This study explores the cooling potential of TFTEC at high temperatures. However, in the actual high temperature environment, the material properties will undergo great changes, and the cooling performance and reliability will also be weakened to a certain extent. It is undoubtedly a challenging task for TFTEC to maintain such high cooling performance under real conditions. In future work, temperature-dependent material properties and operational reliability should be considered in the design.

5. Conclusion

In this paper, we propose a framework for the system level optimization of the TFTEC in 3D electronic packaging based on Taguchi-Grey method. An L_{25} (5^6) orthogonal array is employed to assess the influences of the leg height, the fill-ratio, the electrode height, the gap distance, the hotspot size and the hotspot heat flux on the passive and active cooling effects. The major findings are as follows:

(1) The influence of the six factors on passive cooling effect is ranked as: $h_E > A_{hs} > q_{hs} > h_{TE} > d_{gap} > r_{fill}$. For active cooling, the influence of the six factors is ranked as: $h_E > h_{TE} > d_{gap} > r_{fill} > A_{hs} > q_{hs}$. When the leg height is increased, the passive cooling continues to decrease, whereas the active cooling is increased. There is a trade-off between the mean S/N ratios of the passive cooling and that of the active cooling. Hence, it is necessary to choose the appropriate leg height according to the usage scenario to avoid weakening too much passive cooling, while staying away from the "negative temperature region" where the TFTEC loses its cooling effects.

(2) The fill ratio has a small influence on the passive cooling effect, whereas it has an obvious influence on the active cooling. Increasing the electrode height is beneficial to move away from the "negative temperature region" and simultaneously improve the passive and active cooling. A minimized gap distance is conductive to the cooling effects of the TFTEC. Passive cooling is more sensitive to the hotspot size than active cooling. As the hotspot size is increased, the passive cooling effect can be greatly improved. When the hotspot heat flux is 3000 W/cm^2, i.e., at level 5, the maximum cooling effects can be achieved.

(3) The electrode height (Factor C) is the most important design factor that influenced the passive cooling and active cooling, contributing for 45.5% and 45.3%, respectively. The contribution ratios of hotspot size and hotspot heat flux to passive cooling reach 21.4% and 14.7%, respectively. The contribution ratios of leg height and gap distance to active cooling reach 25.7% and 18.8%, respectively.

(4) The optimum combination (A3, B2, C5, D1, E5 and F5) is obtained by using the Taguchi-Grey method. A passive cooling of 16.82 °C and a maximum active cooling of 12.29 °C are achieved, leading to a total localized cooling of 29.11 °C for a chip hotspot. For a low-power discrete device, TFTEC can reduce its power consumption by up to 23% while consuming 8% of the power. For a high-power multi-chip module, TFTEC can reduce its power consumption by up to 23.2%, while only consuming 3% of the power.

CRediT authorship contribution statement

Tingrui Gong: Conceptualization, Methodology, Formal analysis, Writing – original draft. **Yongjia Wu:** Investigation, Software, Writing – original draft. **Juntao Li:** Writing – review & editing, Formal analysis. **Wenting Lin:** Software, Visualization. **Lei Gao:** Writing – review & editing, Project administration. **Limei Shen:** Writing – review & editing, Validation. **Nan Zhou:** Writing – review & editing. **Tingzhen Ming:** Conceptualization, Investigation, Supervision.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

This study was financially supported by the National Natural Science Foundation of China (NSFC) (Grant No. 52106032), the Science Challenge Program (Grant No. TZ2018003), the Key Research and Design Projects of Hubei Province (Grant No. 2020BAB129), and the Fundamental Research Funds for the Central Universities (WUT: 2021IVA037).

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