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A Strategy to Reduce the Peak Temperature of the Chip Working under Dynamic Power Using the Transient Cooling Effect of the Thin-Film Thermoelectric Cooler

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Abstract: The thin-film thermoelectric cooler (TEC) is a promising solid-state heat pump that can remove the high local heat flux of chips utilizing the Peltier effect. When an electric current pulse is applied to the thin-film TEC, the TEC can achieve an instantaneous lower temperature compared to that created by a steady current. In this paper, we developed a novel strategy to reduce the peak temperature of the chip working under dynamic power, thus making the semiconductor chip operate reliably and efficiently. A three-dimensional numerical model was built to study the transient cooling performance of the thin-film TEC on chips. The effects of parameters, such as the current pulse, the heat flux, the thermoelement length, the number of thermoelements, and the contact resistance on the performance of the thin-film TEC, were investigated. The results showed that when a current pulse of 0.6 A was applied to the thin-film TEC before the peak power of the chip, the peak temperature of the chip was reduced by more than 10°C, making the thin-film thermoelectric cooler a promising technology for the temperature control of modern chips with high peak powers.

Keywords: temperature control, transient cooling, thermoelectric cooler, heat transfer

1. Introduction

The thermoelectric cooler (TEC) is a solid-state heat pump that works based on the Peltier effect. The working temperature of the TEC based on Bi_2Te_3 material ranges from –40°C to 80°C. Since the first thermoelectric refrigerator was designed by Julian Goldsmid in 1953, the cooling performance of the TEC has been improved significantly. Its coefficient of performance (COP), which is the ratio of the thermal output power and the electrical input power, has increased from 0.5 [1, 2] to 1.77 [3] as reported in the literature. Although the COP value of the commercial TEC is still far lower than that of the air-conditioning equipment working based on

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Nomenclatures

c_p	specific heat of fluid at constant pressure/J·kg^{-1}·K^{-1}	T_h	temperature of the heat sink/°C
$\vec{E}$	electric field/V·m^{-1}	∇T	temperature gradient/K·m^{-1}
h	convective heat transfer coefficient/ W·m^{-2}·K^{-1}	T_1	peak temperatures of the chip substrate without a current pulse applied to the thin-film TEC/°C
I	electric current/A	T_2	peak temperatures of the chip substrate with a current pulse applied to the thin-film TEC/°C
$\vec{J}$	current density/A·m^{-2}	W	input electrical power of the thin-film TEC/W
K	thermal conductance of the thin-film TEC/W·K^{-1}	**Greek symbols**	
k	thermal conductivity of the thermoelectric material/W·m^{-1}·K^{-1}	α	Seebeck coefficient/V·K^{-1}
Q_c	cooling capacity/W	α_{pn}	Seebeck coefficient of the junction/V·K^{-1}
Q_h	heating capacity/W	γ	electrical resistivity of the thermoelectric material/Ω·m
$\vec{q}$	heat flux/W·m^{-2}	**Abbreviations**	
q_1	the heat flux of the chip during 0–0.3 s and 0.6–1 s/W·m^{-2}		
q_2	the heat flux of the chip during 0.3–0.6 s/W·m^{-2}	COP	coefficient of performance
R	electrical resistance of the thin-film TEC/Ω	TE	thermoelectric
T	temperature/°C	TEC	thermoelectric cooler
T_c	temperature of the chip substrate/°C	ZT	figure of merit

refrigerant compression, the TEC has been widely used in a variety of small-scale refrigeration applications because it is environmentally friendly, compact, quiet, and highly reliable [4].

The performance of a thermoelectric (TE) material for power generation or cooling is judged by its figure of merit (ZT). Though the ZT values of the thermoelectric materials commercially available are still lower than 2.0, it is believed that there is no physical upper limitation for the ZT value. Since the 1990s [5, 6], the efficiency of TE devices has dramatically increased thanks to the impressive progress in nanomaterials and thermal design technology. Poudel et al. [7] found that a peak ZT of 1.4 was achieved at 100°C in p-type nanocrystalline BiSbTe bulk alloy. Harman et al. [8] reported a peak ZT of 3.5 for Bi-doped n-type PbSeTe/PbTe quantum-dot super-lattice. Scientists devoted tremendous effort to explore nanostructured thermoelectric materials since Dresselhaus [9] pointed out that the ZT value of one-dimensional thermoelectric materials could be higher than 10. However, the promising nanostructured TE materials still failed to meet the industrial needs. It was believed that this was because many manufacturing challenges rather than theoretical analysis still need to be addressed [10].

The structure optimization of the TEC based on thermodynamic analysis is another critical way to improve the performance of the device [11]. More and more attention has been paid to the effective temperature control of electronics by integrating micro-TEC into the device. Taking the semiconductor chips as an example, its processing speed and power density increase explosively with Moore's Law [12, 13]. The peak heat flux even exceeds 1000 W/cm^2 [14, 15], resulting in localized hotspots with extremely high temperatures. Such chip hotspots can seriously affect the performance and reliability of the chip, thus shortening the device's service life [16]. To maintain the chip at a safe temperature, it is necessary to develop advanced thermal management solutions with ultra-high heat dissipation capacity [17]. Cooling technology based on thin-film TEC is a promising candidate. Usually, the cooling power density of the thin-film TEC decreases with the thermoelement length [18]. However, fabricating a thermoelement with a length of 10–50 μm is very difficult. There are two main methods available for thermoelectric material fabrication. One is the conventional method based on cutting and welding assembly of bulk thermoelectric materials made from hot press or SPS [19, 20], which is commonly used in the industry. And another is to deposit the p-type and n-type thin-film thermoelement on the electrics directly by chemical vapor deposition [21], molecular beam epitaxy [22], selective laser melting [23], or thermal spay [24]. There is no doubt that if the chemical vapor deposition method is successfully implemented, large-scale production of thin-film TEC would become a reality. However, the miniaturization of TEC is influenced by the

electrical and thermal contact resistance at the TEC interfaces [25]. In the thermoelectric module with the thermoelement length of tens of micrometers, the irreversible loss caused by the electrical and thermal contact resistance is significant enough to offset the cooling capacity, which plays a dominant role in affecting the performance of thin-film TEC. Until now, the lowest electrical contact resistance reported in the literature is on the order of 10^{-6} $\Omega\cdot cm^2$ for the thin-film TEC [5]. To further improve the cooling capacity of TEC, it is necessary to further reduce the electrical contact resistance. When the electrical contact resistance is reduced to a magnitude of 10^{-7} $\Omega\cdot cm^2$, the thin-film TEC with a thermoelement length of 25–60 μm can create a maximum temperature difference of 60°C and a maximum cooling capacity of 500 W/cm^2 [1]. When the thermoelement length drops below 25 μm, both the electrical and thermal contact resistance can jointly affect the cooling performance of the thin-film TEC. The thermal contact resistance in the thin-film TEC has been reduced to the magnitude of 10^{-7} $K\cdot m^2\cdot W^{-1}$ in the most recent work reported by Chen [26]. According to the theoretical calculation based on phonon transport [26], the lowest thermal contact resistance is in the order of 10^{-8} $K\cdot m^2\cdot W^{-1}$. Only in this situation, a meaningful cooling capacity can be achieved by the thin-film TEC with a thermoelement length below 25 μm. With the improvement in material engineering, manufacturing process and device design, the implementation of thin-film TEC in the modern chip for temperature control becomes a reality. Chowdhury et al. [15] reported that a heat flux of around 1300 W/cm^2 and a temperature drop of 7.3°C could be achieved by a thin-film TEC made by ultra-thin superlattice thermoelectric materials.

If a current pulse being several times higher than the steady-state current was applied to the TEC, an instantaneous lower temperature compared to that created by a steady current can be obtained at the cold end of the device due to the delay of the thermal conduction of the Joule heat [27]. It is found that transient current pulse through the TEC can achieve larger degree of cooling than steady state current [28], and current pulse of varying shapes through the TEC can largely affect the temperature of the attached chip. Various methods, such as the application of variable transient current [29], variable cross-sectional area of thermoelement [30], and segment thermoelectric modules [26], have been adopted to explore the characteristics of the transient cooling effect. In recent years, using the transient cooling effect to reduce the peak temperature of the chip has provoked the great interest of many researchers. Snyder et al. [29] established both theoretical and experimental essential parameters to describe the transient cooling effect, such as the minimum temperature achieved, maximum temperature overshoot. Shen et al. [31] found that the minimum transient cooling temperature cannot approach absolute zero as reported in previous research due to the co-existence of the Joule heat and Peltier effect. Lv et al. [32] investigated various current pulses to search for the optimal current shape; the results showed that the optimal shape was only determined by the time to reach the minimum cold-end temperature and the current pulse width. When the chip works at a power near to the peak value, the heat flux generated by the chip can reach to 500 W/cm^2 [33]. Sullivan et al. [34] analyzed the operation of multiple TECs for cooling spatiotemporal hot spots in microprocessors. The analysis shows that the transient cooling with a high amplitude current pulse is beneficial to the short-term and infrequent hot spots. In this situation, the transient cooling effect of the thin-film TEC can be used to reduce the peak temperature of the chip. Some researchers studied the influence of transient cooling of bulk TEC on the peak temperature and thermal stress in the chip [35–38]. It has been found that the peak temperature of the chip could reduce by 10°C–20°C, which has a significant impact on the performance of the chip. However, the utilization of thin-film TEC for controlling the temperature of the modern chips has not been fully explored (Fig. 1).

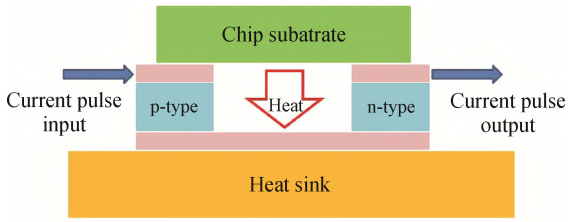

Fig. 1 Reduce the peak temperature of the chip under dynamic power using thin-film TEC

Because the progress to reduce the thermal and electrical contact resistance was very slow in the past two decades, using the transient cooling effect of thin-film TEC for continuous electronics cooling has been thought unpractical [36]. Thus, many researchers have switched their interests to other cooling technologies. However, using the transient cooling effect to control the peak temperature of the chip working under dynamic power may become practical and has commercial potential. In this paper, we built a comprehensive three-dimensional numerical model to study the temperature control performance of a thin-film TEC taking advantage of its transient cooling effect. The influence of the parameters, such as the current pulse, the heat flux, the thermoelement length, thermoelement numbers, and the thermal contact conductivity, on the performance of the thin-film TEC was systematically investigated. The mechanisms how the Peltier effect, Joule effect, and interface contact resistance affect the transient cooling

effect were analyzed. Our research results provide a useful guide for the design and fabrication of high-performance thin-film TEC employed for controlling the peak temperature of modern chips working under dynamic power.

2. Model Description

2.1 Geometric model

As illustrated in Fig. 2, a chip substrate (SiC) with dimensions of 1400×1400×300 μm^3 is attached to the cold end of a thin-film TEC. The TEC consists of 8 pairs of thermoelements which are connected electrically in series and thermally in parallel. The size of each thermoelement is 200×200×20 μm^3. The Bi_2Te_3-based material is used for the p-type and n-type thermoelements since its ZT value is among one of the highest for the thermoelectric materials working at the room temperatures. The copper slice with thickness of 5 μm is used as the electrode due to its high electrical and thermal conductivity. Aluminum oxide ceramic plates with a thickness of 2 μm are bonded to the both ends of the thermoelements for electrical isolation. A copper heat sink with dimensions of 2500×2500×400 μm^3 is attached to the hot-end of the thin-film TEC. The critical parameters of the thin-film TEC are summarized and listed in Table 1. The properties of the materials used in the numerical model are presented in Fig. 2 and Fig. 3.

Table 1 Basic parameters of the thin-film TEC

The parameters	Dimensions
Heat sink thickness/μm	400
Thermoelement length/μm	20
Copper slices thickness/μm	5
Ceramic plate thickness/μm	2
Chip substrate thickness/μm	130
Thermoelement gap distance/μm	200
Cross-sectional area of the chip/μm^2	1400×1400
Cross-sectional area of the substrate/μm^2	2500×2500
Cross-sectional area of the thermoelement/μm^2	200×200

Table 2 Material properties used for the modeling [39, 40]

Material	Material properties	Material properties
Cu	Thermal conductivity/W·m^{-1}·K^{-1}	398
	Electrical conductivity/Ω·m	1.8×10^{-7}
SiC	Thermal conductivity/W·m^{-1}·K^{-1}	450
Al_2O_3	Thermal conductivity/Ω·m	37.2

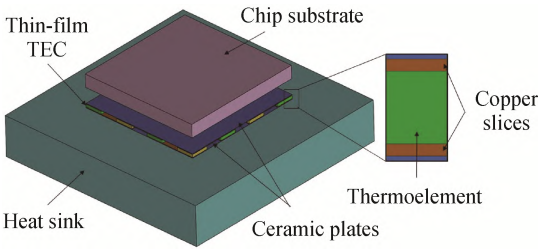

Fig. 2 Geometric model of the thin-film TEC on-chip

2.2 Mathematical model

The continuity equation in the vector form for a constant current is given by [41]

$$\nabla \cdot \vec{J} = 0 \tag{1}$$

where the vector $\vec{J}$ represents the current density.

The electric field $\vec{E}$ is influenced by the current density $\vec{J}$ and the temperature gradient (or the Seebeck effect) ∇T where T is the temperature. The electric field is expressed as

$$\vec{E} = \vec{J}\gamma + \alpha \nabla T \tag{2}$$

where α is the Seebeck coefficient, and γ represents electrical resistivity.

The energy conservation equation for the thermoelectric material is given by

$$\dot{q} - \nabla \cdot \vec{q} = \rho c_p \frac{\partial T}{\partial t} \tag{3}$$

where $\dot{q}$, c_p, and $\partial T/\partial t$ are the heat generated per unit volume, the specific heat capacity, and the change rate of the temperature, respectively.

The $\dot{q}$ in Eq. (3) can be rewritten as

$$\dot{q} = \vec{E} \cdot \vec{J} = \vec{J}^2 \gamma + \vec{J} \cdot \alpha \nabla T \tag{4}$$

Though the thin-film TEC module is micron scale, the heat transfer is still in the macroscopic range. The heat flux $\vec{q}$ in the TEC can be calculated by

$$\vec{q} = \alpha T \vec{J} - k \nabla T \tag{5}$$

where k represents thermal conductivity. The term $\alpha T\vec{J}$ indicates the Peltier heat, and the term $k\nabla T$ refers to Fourier heat.

Substituting Eqs. (4) and (5) into Eq. (3), the transient energy governing equation coupling the temperature T and electrical current density can be expressed as [42]

$$\nabla \cdot \left(k \nabla T\right) + \gamma \vec{J}^2 - T \frac{\partial \alpha}{\alpha T} \vec{j} \cdot \nabla T = \rho c_p \frac{\partial T}{\partial t} \tag{6}$$

where k, γ, and α are functions of temperature. The first term of Eq. (6) describes the thermal conduction; the second term refers to the Joule heat, and the third term represents the Thomson heat.

As shown in Fig. 3, delivering the current I to the thin-film TEC results in the heat absorbed at the cold-end and released at the hot-end [3]:

$$Q_c = \alpha_{pn} I T_c - \frac{I^2 R}{2} - K\left(T_h - T_c\right) \tag{7}$$

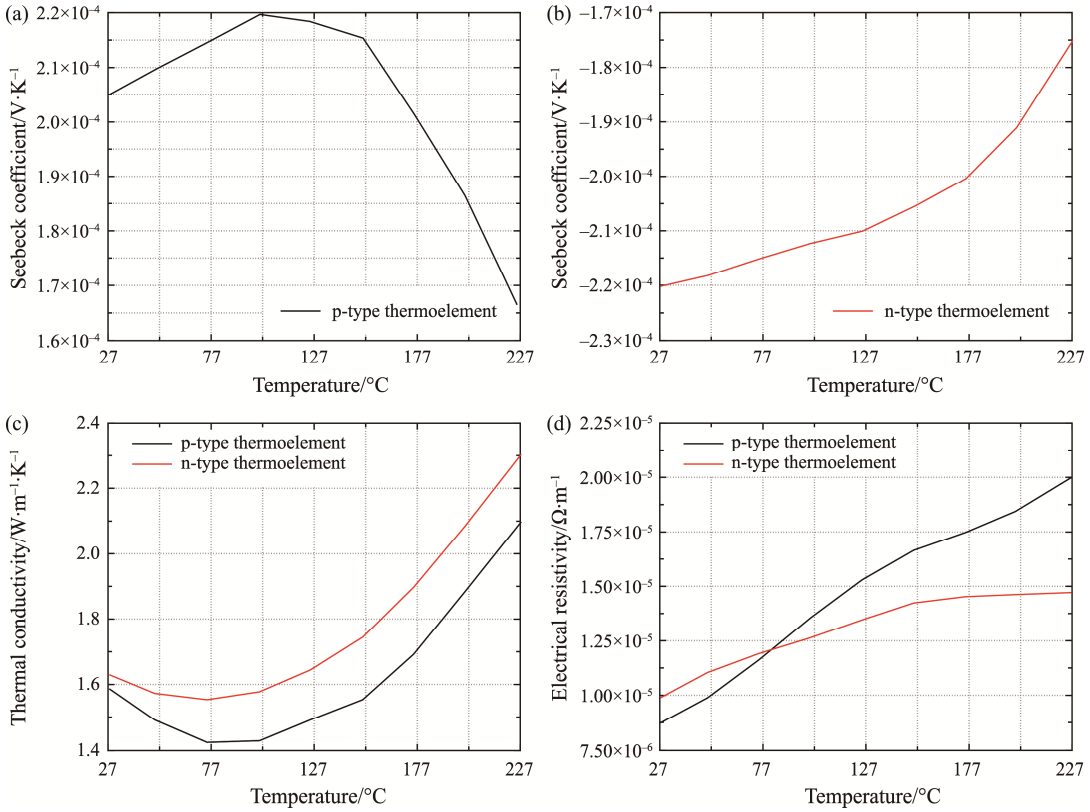

Fig. 3 Temperature dependent materials properties: (a) Seebeak coefficient of p-type thermolelment varying with temperature; (b) Seebeak coefficient of n-type thermolelment varying with temperature; (c) Thermal conductivity of p-type and n-type thermoelement varying with temperature; (d) Resistivity coefficient of p-type and n-type thermoelement varying with temperature

$$Q_h = \alpha_{pn} I T_h + \frac{I^2 R}{2} - K\left(T_h - T_c\right) \tag{8}$$

where the α_{pn} is the Seebeck coefficient of the junction for p-type and n-type thermoelements. The first, the second, and the third terms in Eqs. (7) and (8) are the Peltier heat, Joule heat, and Fourier heat, respectively. Note that Peltier effect is reversible, but Joule heating and Fourier heat conduction are irreversible.

According to the first law of thermodynamics, the power consumed by the thin-film TEC equal to the difference between released and absorbed heat [41], which is given by

$$W = Q_h - Q_c = \alpha_{pn} I\left(T_h - T_c\right) + I^2 R \tag{9}$$

Thus, the COP of the thin-film TEC is

$$\mathrm{COP} = Q_c / W \tag{10}$$

2.3 Boundary conditions

Some assumptions are made to simplify the mathematical model with minimal impacts on the results.

(a) All the surfaces except the hot and the cold-ends of the thin-film TEC are assumed to be thermally insulated.

(b) Radiation heat losses from all the surfaces are ignored.

A chip working under dynamic power is attached to the cold-end of the thin-film TEC. The heat flux of the chip consists of three periods to imitate a real situation. As shown in Fig. 5, the heat flux of the chip is q_1 during 0–0.3 s and 0.5–1.0 s, q_2 during 0.3–0.5 s. A current pulse is applied to the thin-film TEC to cool the chip. The current pulse also consists of three periods. The current pulse applied to the thin-film TEC is 0 A during 0–0.45 s and 0.65–0.1 s, 0.6 A during 0.45–0.65 s. The current pulse starts slightly later than the power pulse and ends later than the power pulse because it takes time for the heat to influence the temperature of the chip.

The substrate at the hot end of the thin-film TEC is cooled by water. The convective heat transfer coefficient on the substrate surface is assumed to be 300 W·cm^{-2} [43, 44], which is a typical value commonly adopted for the thermal design of the electronics. The ambient temperature is set as 25°C.

2.4 Numerical methods

In this paper, the numerical simulations are conducted using ANSYS Workbench 19.0 based on the finite element method. To examine the grid-independence, four grid systems with grid numbers of 14 233, 35 837,

87 803 and 152 380, respectively, are tested under the same boundary conditions. It can be seen from Fig. 6 that the temperatures on the surface of the chip are almost identical for the four grid systems, which indicates that the numerical results are independent of the grid systems. In this paper, a grid number of 35 837 is selected to perform the numerical analysis.

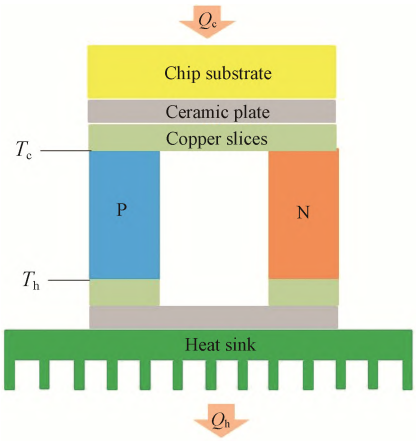

Fig. 4 Basic unit structure of the thin-film TEC (Not drawn to scale)

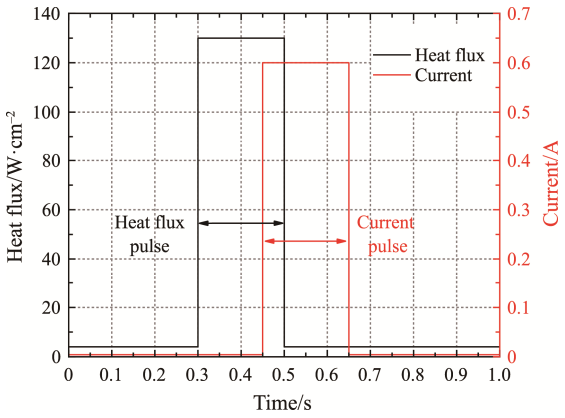

Fig. 5 The heat flux pulse and the current pulse

3. Results and Discussion

The modern chip generates tremendous heat in a short period when working under peak power. If a current pulse is applied to the thin-film TEC before the peak temperature of the chip arrives, a lower temperature of the chip (or TEC) compared to that created by a constant current can be achieved. This phenomenon happens because the Peltier effect is a surface effect while the Joule heating and Fourier heat conduction are volumetric effects. The Peltier effect transfers the heat from the cold end to the hot end of the TEC instantaneously, while it takes time for the heat to diffuse back to the cold end of the TEC, thus creating a momentary low temperature in the cold end of the TEC. This phenomenon is also called supercooling in the literatures [27, 45]. In this section, the critical factors that affect the cooling performance of the thin-film TEC are studied by examining the parameters, including the current pulse, the heat flux, the thermoelement length, the number of thermoelements, and the contact resistance, respectively. We tried to provide a full picture illustrating how the thin-film TEC can reduce the peak temperature of a modern chip.

3.1 Effects of current pulse on the temperature of the chip

The thin-film TEC is regarded as a solid-state heat pump whose cooling capacity is directly affected by the applied current pulse. In this part, the heat flux is 130 W·cm^{-2} during 0.3–0.5 s, and 1 W·cm^{-2} during 0–0.3 s and 0.5–1 s. Fig. 6 shows the temperature profiles of the chip with various current pulses. When the working power pulse being higher than the average power is applied on the chip suddenly, the heat flux generated by the chip changes immediately. This causes a rapid temperature rise within the chip during the pulse duration. The temperature of the chip continuously increases until it reaches the peak value at the end of the power pulse.

As shown in Fig. 7, when no current passes through the thin-film TEC, the temperature of the chip keeps rising until reaching the peak value of 123.6°C with a power pulse of 130 W·cm^{-2}. With a current pulse applied during 0.45–0.65 s, the temperature of the chip drops significantly due to the Peltier effect. Near to the end of the current pulse, the temperature of the chip starts to increase again. This happens because the Joule heat and the Fourier heat conduction offset the Peltier effect. With the current increasing from 0 A to 0.8 A, the peak temperature of the chip is reduced from 123.6°C to 113.4°C. The temperature drop of the chip is not apparent

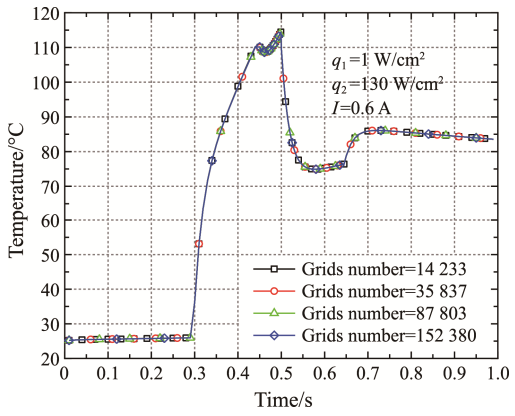

Fig. 6 Comparison of temperature profiles with four different grid systems

when the current magnitude is small because the Peltier effect is weak. However, when the current pulse exceeds a certain threshold, the transient cooling performance of the thin-film TEC becomes worse. It even does not function when the current pulse is more than 1.3 A. This is because the summation of the Joule heat and Fourier heat is larger than the heat removed by the Peltier effect. At the end of the current pulse at 0.65 s, the temperature of the chip starts to increase due to the Fourier heat transfer from the hot end to the cold end of the thin-film TEC.

The transient cooling performance is evaluated by the drop of the peak temperature of the chip, $\Delta T=T_1-T_2$, where T_1 and T_2 are the peak temperatures of the chip without/with a current pulse, respectively. As presented in Fig. 8, the ΔT is 4.1°C, 7.1°C, 9.2°C, 10.3°C, 10.3°C, 9.4°C when the current is 0.2 A, 0.4 A, 0.6 A, 0.8 A, 1.1 A and 1.3 A, respectively. The ΔT increases until the applied current pulse is higher than 1.1 A. This is because the Peltier effect plays a dominant role when the applied current pulse is small. However, the variation trend of ΔT versus the applied current pulse reverses as it reaches to 1.1 A, where the influence of the Joule heating becomes more significant.

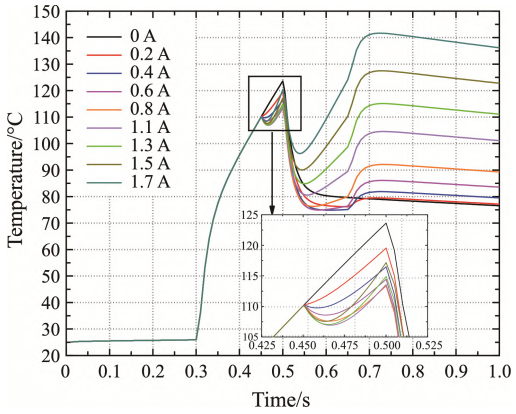

Fig. 7 Temperature variations of the chip with different current pulses

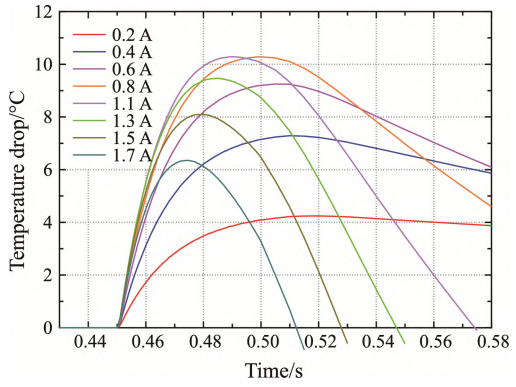

Fig. 8 The peak temperature drops of the chip with different current pulses

3.2 Effects of heat flux on the temperature of the chip

Fig. 9 demonstrates the effects of heat flux pulse on the temperature of the chip. The heat flux pulse consisted of three periods. The heat flux of the chip is q_1=1 W·cm^{-2} during 0–0.3 s and 0.5–1.0 s, and q_2=100–130 W·cm^{-2} during 0.3–0.5 s, which is set according to the power of commercial 5G chips. A current pulse of 0.6 A is applied to remove the heat generated by the chip. As shown in Fig. 9, the temperature of the chip increases with the heat flux.

The transient cooling performance was evaluated by the drop in the peak temperature (ΔT) of the chip. The ΔT increases persistently from 0°C at 0.45 s to the maximum value at 0.5 s, and then starts to decrease from 0.65 s. With the heat flux varying from 100 W·cm^{-2} to 130 W·cm^{-2} at an interval of 10 W·cm^{-2}, the peak temperatures of the chip reduce by 8.62°C, 8.69°C, 9.11°C, and 9.25°C respectively, as shown in Fig. 10. The temperature drop in the chip is more significant for the case with higher heat flux. The silicon-based chip can only work normally with a peak temperature lower than 120.0°C; a peak temperature drop by 8°C–10°C will significantly improve the reliability and performance of the modern chip [46].

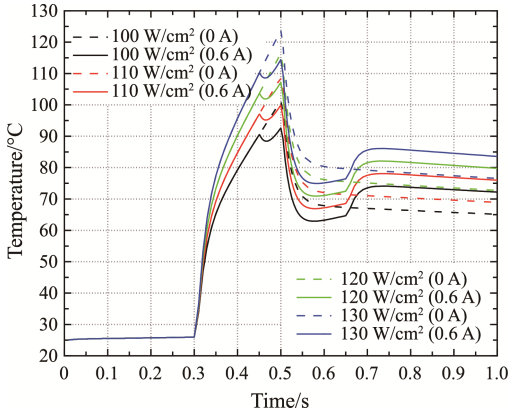

Fig. 9 Temperature variations of the chip with different heat fluxes

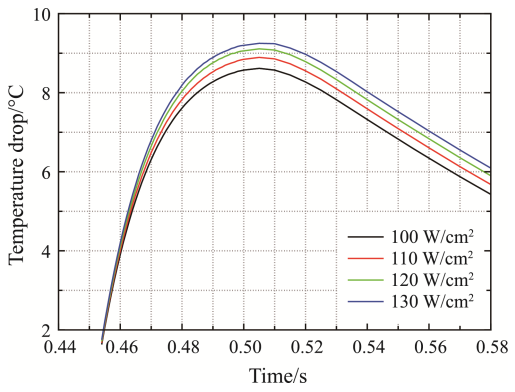

Fig. 10 The peak temperature drops of the chip with different heat fluxes

3.3 Effects of thermoelement length on the temperature of the chip

The transient cooling performance of the thin-film TECs with thermoelement lengths of 20 μm, 25 μm, 30 μm, 35 μm, and 40 μm are studied. Fig. 11 shows the temperature variations of the chips with different thermoelement lengths working with a heat flux of 130 W/cm^2. It is found that the longer the thermoelement, the higher the temperature of the chip will be. The drops in the peak temperatures of the TEC with different thermoelement lengths are illustrated in Fig. 12. With a current pulse of 0.6 A applied to the thin-film TEC, the peak temperatures of the chips with thermoelement lengths of 20 μm, 25 μm, 30 μm, 35 μm, and 40 μm reduce 9.2°C, 11.6°C, 13.9°C, 16.1°C, and 18.2°C respectively. Fig. 11 also shows that ΔT increases with the length of thermoelement. However, the longer thermoelement results in a higher average temperature of the chip, which worsens the working environment of the chip. To ease this contradiction, the thermal mass of the substrate should be increased to store the Joule heat temporarily generated by the thin-film TEC, like the situation in the 5G mobile phone where the chip is directly connected to the back cover by ultra-thin flat heat pipes or interface materials with high thermal conductivities. In this case, a high current pulse, such as 5.0 A, can be employed to create a considerable temperature drop.

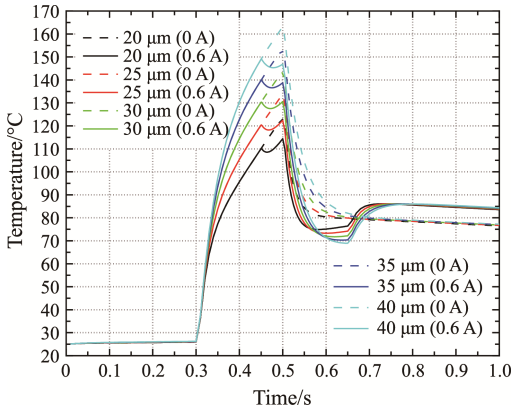

Fig. 11 Temperature variations of the chip with different thermoelement lengths

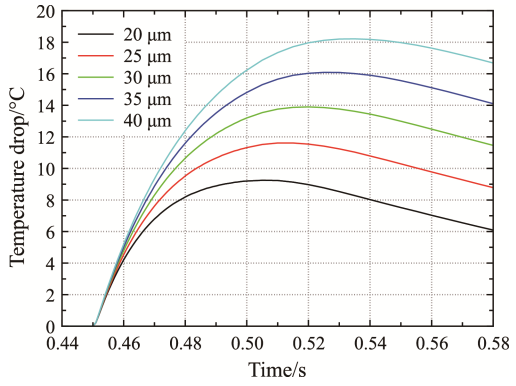

Fig. 12 The peak temperature drops of the chip with different thermoelement lengths

3.4 Effects of thermoelement number on the temperature of the chip

The thermal behaviors of the thin-film TEC with different thermoelement numbers were studied in this section. The geometries of all the thermoelements are identical as illustrated in Table 1. Three-dimensional numerical modeling is undertaken to predict the transient cooling performance of the thin-film TEC working under a heat flux of 130 W/cm^2. Fig. 13 presents the temperature profiles of the chip with different thermoelement numbers. The temperature of the chip significantly decreases with the increasing thermoelement numbers. The total cross-sectional area and the filling ratio are larger for TEC with more thermoelements, which results in a decrease in the average heat fluxes exerted on each thermoelement. As discussed in Section 3.2, the temperature of the chip decreases with a small heat flux. The increase of thermoelement numbers ultimately improves the cooling performance of the thin-film TEC. Fig. 13 also shows that the temperature of the chip recovers quicker after the current pulse with the TEC with more thermoelements because the thermal resistance of the thin-film TEC is reduced. As long as the second peak temperature of the TEC is lower than the first peak, we can draw the conclusion that the transient cooling performances of the thin-film TEC are expected to be enhanced with more thermoelements.

Fig. 14 shows the variation of ΔT with different thermoelement numbers. The peak temperature of the chip reduces by 6.2°C, 9.1°C, and 10.0°C when the thermoelement numbers are 9, 16, and 25, respectively. More considerable temperature drop is observed for the case with a larger thermoelement number. It is also found that the maximum temperature drop occurred earlier for the case with more thermoelements. It can be reasoned by the decrease in the time constant of the thin-film TEC.

Fig. 15 presents the COP of the thin-film TEC with different thermoelement numbers. The applied current is 0.6 A during 0.45 s–0.065 s. When the temperature of the chip is increasing, the COP changes slightly and is much higher than the COP when the temperature of the chip is decreasing. The maximum COPs are 1.4, 0.9, and 0.4 for the thermoelement numbers are 9, 16, and 25, respectively. It is found that the COP is larger with less thermoelement numbers.

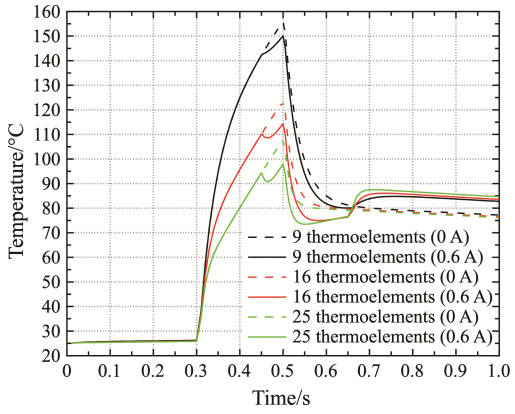

Fig. 13 Temperature variations of the chip with different thermoelement numbers

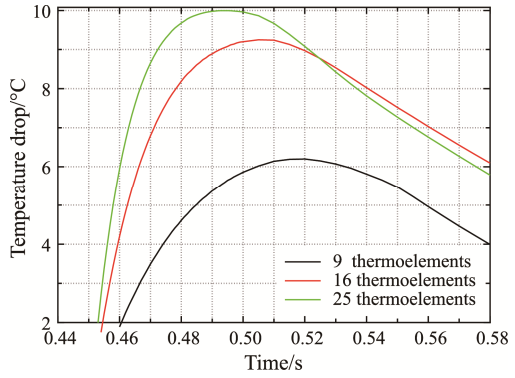

Fig. 14 The peak temperature drops of the chip with different thermoelement numbers

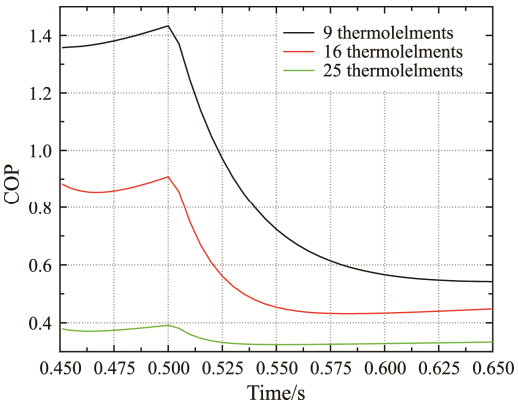

Fig. 15 The COP of the thin-film TEC with different thermoelement numbers

3.5 Effects of interfacial contact thermal resistance on the temperature of the chip

The electrical and thermal contact resistances between the metal and semiconductor interfaces dramatically influence the cooling capacity of the thin-film TEC. The tremendous effort has been made to explore new methods for the fabrication of thin-film TECs. Recently, Xiang et al. [47] reported that the lattice matching between Cu and $Bi_2Te_{2.7}Se_{0.3}$ can significantly reduce the electrical and thermal contact resistance. Though much progress has been made in the past two decades, the parasitic contact resistance is still a prominent issue for the thin-film TEC. The electrical contact resistivity between the copper electrode and nanostructured Bi_2Te_3-based thermoelectric materials was reported in the order of 1.25×10^{-6} $\Omega\cdot cm^2$ [48–50]. According to the calculation conducted by Chen [26] based on the interfacial phonon transmission theory, the thermal contact resistance was on the magnitude of 10^{-9}–10^{-8} $K\cdot m^2\cdot W^{-1}$ for a perfect interface. Previous research found that the impacts of thermal contact resistance on the performance of the thin-film TEC are more significant than that of the electrical contact resistance [51].

This paper mainly studied the influence of thermal contact resistance on the transient cooling performances of the thin-film TEC with the thermal contact resistivities of 8×10^{-8} $K\cdot m^2\cdot W^{-1}$ (theoretical limit value), 1.6×10^{-8} $K\cdot m^2\cdot W^{-1}$, 6×10^{-7} $K\cdot m^2\cdot W^{-1}$, 8.3×10^{-7} $K\cdot m^2\cdot W^{-1}$, 1.25×10^{-6} $K\cdot m^2\cdot W^{-1}$, 1.42×10^{-6} $K\cdot m^2\cdot W^{-1}$, 2×10^{-6} $K\cdot m^2\cdot W^{-1}$, respectively. Fig. 16 shows the effects of thermal contact conductivity on the cooling performance of the thin-film TEC with an applied current pulse of 0.6 A and a heat flux pulse of 130 $W\cdot cm^{-2}$. The temperature of the chip increases with increasing the thermal contact resistivity, which indicates that the cooling capacity of the thin-film TEC is reduced due to the increased thermal contact resistivity. To find out the threshold of the thermal contact resistivity, the temperature profiles for the cases with different contact resistivities are compared. When the thermal contact resistivity is 1.25×10^{-6} $K\cdot m^2\cdot W^{-1}$, the cooling effect of the thin-film TEC is almost offset by the contact thermal resistance. It is critical to reduce the thermal contact resistivity to enhance the cooling performance of the thin-film TEC.

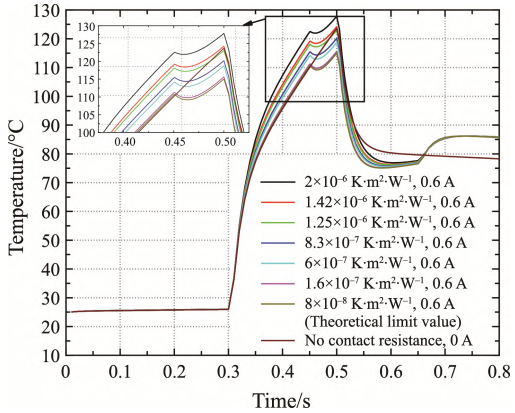

Fig. 16 Temperature variations of the chip with different thermal contact resistivities

3.6 Cooling effects of the thin-film TEC on the temperature of the chip

In this section, we conducted a numerical simulation based on the geometric model that the chip substrate is directly attached to the heat sink, as seen in Fig. 17. The thermal contact resistivities between the chip and semiconductor interfaces are considered. To figure out the range of the thermal contact resistivities that the thin-film TEC has a better cooling performance, the active cooling effect of the thin-film TEC is compared with the passive cooling effect of the heat sink, as seen in Fig. 18. The larger the thermal contact resistivities, the higher the temperature of the chip; this is because larger thermal contact resistivities hinder heat transfer from the chip to the heat sink preferably.

When the thermal contact resistivities between the chip and semiconductor interfaces are 4×10^{-5} K·m^2·W^{-1}, the temperature of the chip is almost identical to the temperature of the chip that there is no current applied to the thin-film TEC. As the thermal contact resistivities are 3×10^{-5} K·m^2·W^{-1}, the peak temperature of the chip is equal to the peak temperature of the chip that the optimal current applied to the thin-film TEC. Thus, if the thermal contact resistivities are lower than 3×10^{-5} K·m^2·W^{-1}, the passive cooling effect of the heat sink is better than the active cooling effect of the thin-film TEC.

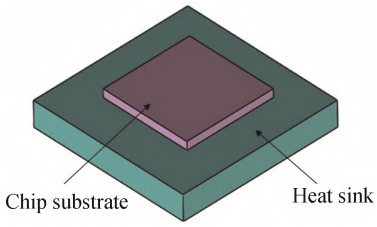

Fig. 17 The geometric model without thin-film TEC

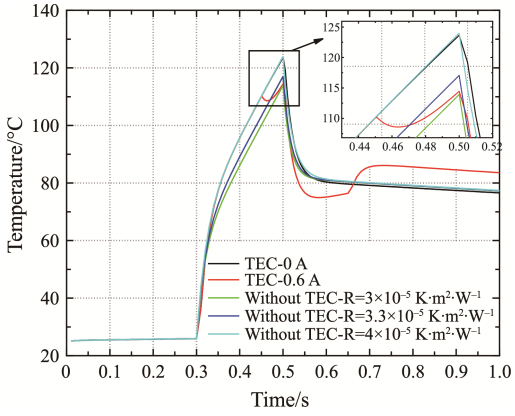

Fig. 18 Range of the thermal contact resistivities when chip substrate attached to the heat sink

4. Conclusions

In this paper, we proposed a novel strategy to reduce the peak temperature of the chip working under dynamic power using the transient cooling effect of the thin-film TEC. The effects of the current pulse amplitude, heat flux, thermoelement length, thermoelement number, and thermal contact conductivity on the cooling performance of thin-film TEC were systematically studied by a multi-physics numerical model. The following conclusions can be drawn from the results:

The cooling performance of the thin-film TEC was improved by increasing the current from 0 to 0.6 A. The peak temperature of the thin-film TEC could be reduced by more than 10°C when the current pulse was between 0.6 A and 0.8 A, which had the potential to improve the reliability and performance of the silicon-based chip. Once the current pulse exceeded the critical value, the cooling performance of the thin-film TEC was gradually reduced. When the current pulse was more than 1.3 A, the TEC lost the cooling function.

The higher the heat flux passing through the thin-film TEC, the larger the temperature drop that could be made by the thin-film TEC. Though the peak temperature of the chip increased with the thermoelement length, the thin-film TEC with a longer thermoelement could create a larger temperature drop. In addition, the temperature of the chip reduced significantly with the thermoelement number.

With the increase of thermal contact resistivity, the cooling capacity of the thin-film TEC weakened dramatically. Once the thermal contact resistivity was higher than 1.25×10^{-6} K·m^2·W^{-1}, the thin-film TEC lost its cooling function.

Using the transient cooling function of the thin-film TEC to control chip's temperature provides many opportunities for the design of next-generation high-performance chips. Experimental validation is undertaking to validate the simulated performance of the chip integrated with the thin-film TEC.

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